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High-Temperature Electrical Characterization of $Ge_2Sb_2Te_5$ Phase Change Memory Devices

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Faruk Dirisaglik, Ph.D.

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Phase change memory (PCM) is one of the most promising non-volatile memory technologies in the marketplace today and offers tremendous potential for high speed, energy efficient computing as a non-volatile DRAM replacement or as a direct competitor to flash memory. PCM devices utilize the electrical resistivity contrast between highly resistive amorphous and highly conductive crystalline phases of phase change materials. Their operation differs significantly from conventional solid state devices: PCM devices experience melting, resolidification and crystallization in nanosecond time scales, with high current densities and strong thermal gradients. Understanding threshold switching, crystallization dynamics, resistance drift phenomena, and electrical and thermal transport in nanoscale, in conjunction with complete modeling, will significantly accelerate PCM development. Detailed characterization of material properties in the device operation time scales for a wide temperature range is critically important.

In this work, the impacts of the material parameters and thermoelectric effects are illustrated using finite element modeling. Temperature dependent electrical resistivities of the metastable amorphous and fcc (face centered cubic) phases of $Ge_2Sb_2Te_5$ (GST-the

most common phase change material) are measured for the first time in nanoscale device level (PCM line cells) using the high-speed electrical pump-probe characterization technique developed for this work. Electrical resistivities of liquid and hcp (hexagonal close packed) phases are also measured with the same measurement technique. In addition to these, crystallization processes immediately after amorphization are monitored at elevated temperatures and resistance drift behaviors in amorphous phase are observed in short (~2 ms) and very long (~13 months) time scales in a 300-675 K temperature range. Electrical breakdown field of amorphous GST is extracted. Carrier density and mobility are measured using the van der Pauw Hall measurement technique for various crystallinity states. The devices are cycled to demonstrate memory operation.

Our studies show that electrical resistivities of metastable amorphous and fcc GST exponentially decrease as a function of temperature with significantly higher values compared to those of the typical slow *R-T* measurements. Crystallization dynamics play a significant role in both resistance drift and carrier activation. Results suggest that nucleation reduces the carrier lifetimes by increasing the trapping probability and charging of these crystalline nuclei gives rise to Coulomb blockade, significantly hindering transport.

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Doctor of Philosophy Dissertation

High-Temperature Electrical Characterization of $Ge_2Sb_2Te_5$ Phase Change Memory Devices

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Table of Contents

List of Figures

List of Tables

1. Introduction

The nature of storing information evolved gradually over time with new technologies such as photochemical storage, magnetic storage, and optical storage to solid state electronic storage which is driven by the semiconductor industry. Currently, flash memory, which can store data for $\geq$ 10 years without power (non-volatile) and DRAM, which can store information temporarily for random access during computation (volatile), are the main solid state storage devices. Due to increasing demand for higher speed and larger storage capacity, the global memory market is looking for new non-volatile memory technologies as scalable as flash memory and as fast as DRAM to replace them respectively. One of the strongest candidates is phase change memory (PCM) (Figure 1.1).

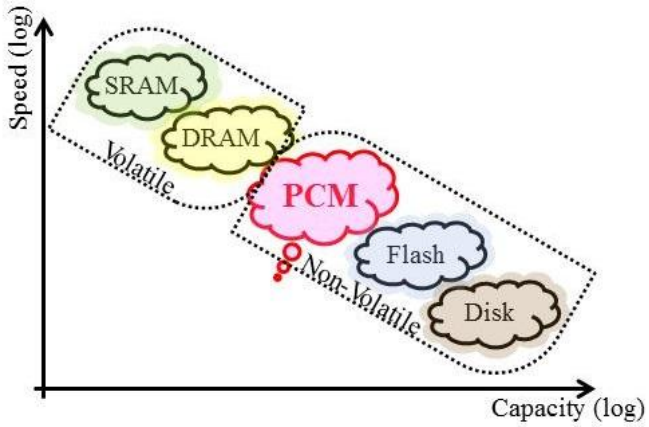


Figure 1.1. Comparison of main digital storage technologies.

PCM, a recent addition to the electronic device technologies in the marketplace, is a high-speed non-volatile memory technology that utilizes a group of compound

materials -chalcogenide alloys- with large resistivity contrast between their highly resistive amorphous and highly conductive crystalline phases. Reversible phase change is achieved by melting and sudden quenching (reset), resulting in the amorphous state and by heating without melting or melting and slowly cooling (set) to reach the crystalline state (Figure 1.2). The same class of materials has been used for rewritable optical disks which utilize the optical reflectivity contrast between amorphous (low reflectivity) and crystalline (high reflectivity) phases, accompanied with the contrast in electrical resistivity. Fully electronic PCM can deliver the speed necessary to be used as a non-volatile random access memory (RAM), resulting in significant power savings, increased reliability and reduced cost. PCM technology also offers the possibility to integrate 100s of gigabytes of embedded non-volatile RAM with the CPU in the same package and practically eliminate all memory access latencies, speeding up computation by > 1000x and reduce the power consumption for most operations [1-14]. However, further engineering of materials and device structures, their characterization and comprehensive modeling of these devices are required to reach endurance of ~10^{15} cycles (5 years of continuous reliable operation as RAM).

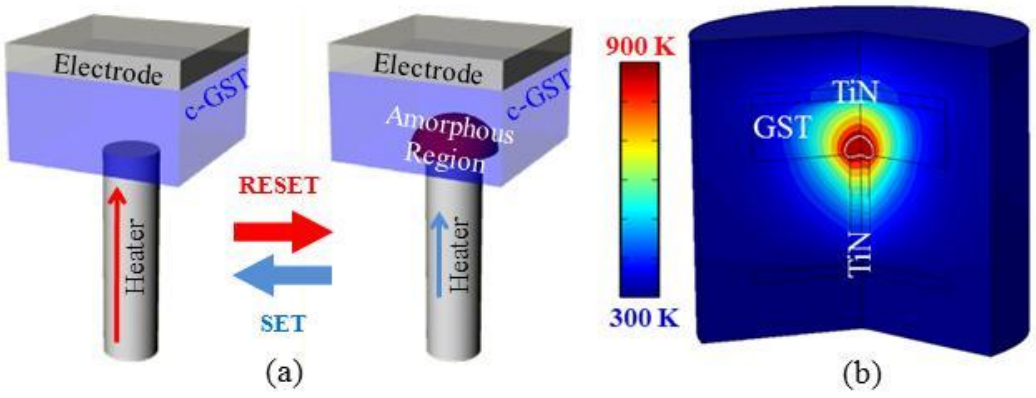


Figure 1.2. Schematic view showing operation (a) and simulated temperature profile (b) of typical mushroom type PCM cells.

PCM falls under the general category of resistive memory (RRAM) and typically consists of an access device such as a transistor or a diode in addition to the two-terminal memory element (a small volume of phase-change material between two contacts). At least one of the contacts made to the phase change material is very small (10-50 nm scale) to confine the current, hence limit the power consumption and increase packing density [4, 5, 7, 15]. Self-heating by passing current through the memory element is utilized for set and reset operations (Figure 1.2a,b). In contrast to conventional electronic devices, which always remain in solid state and operate in a relatively narrow temperature window, PCM devices operate in a temperature range of 300~1000 K and experience melting, resolidification and crystallization in < 1 μs, with high current densities and strong thermal gradients forming within the devices. The crystallization time scale of $Ge_2Sb_2Te_5$ (GST) -the most common phase change material- ranges from > 10 years at room temperature to ~100 ns close to melting temperature ($T_{melt\text{-}GST}$ ~900 K) [2-7, 16, 17] with maximum growth velocity of ~1 m/s [18]. However, during set operation, the temperature increases quickly (~100 ns) and the amorphous region does not have sufficient time for rearrangement of the atoms into a crystalline structure. Hence, amorphous GST (a-GST) retains its metastable amorphous state up to the melting temperature. Similarly, the metastable crystalline fcc (face centered cubic) retains its metastable fcc phase above the fcc-hcp (hexagonal close packed) phase transition during reset operation [19-25]. Additionally, the resistance of the amorphous material increases over time (referred to resistance drift) which affects data retention in long term [2, 3, 5, 6, 26-30]

Although rapid increase in experimental investigations and extensive modeling studies on PCM in the last decade, high temperature electrical and thermal characterization, metastable material properties, crystallization dynamics, and resistance drift phenomena are still elusive [3, 14].

1.1 Current status of characterization of phase change memory devices

The phase change material properties strongly depend on the phase and temperature of the material. Materials used in PCM technology have been characterized in form of bulk, thin films and various device structures such as vertical (mushroom, pore, confined cells) and lateral (line, dog bone, wedge and T shape) devices using electrical and optical characterization techniques as reported in literature [2, 3, 10, 20, 31-35].

Typically, slow and highly sensitive DC current-voltage (*I*-*V*) measurements are performed to characterize the materials electrically. However, phase change materials gradually crystallize as the temperature of a hot-chuck is ramped up (typical ramp rate of ~1 K/min) above the transition temperature during this typical slow resistance versus temperature (*R*-*T*) measurements. Hence, this characterization technique is limited with the transition temperature of the materials and cannot capture the metastable material properties at elevated temperatures. The optical pump-probe techniques, based on the optical reflectivity contrast of these materials using laser pulses are fast and give insight about crystalline fraction but do not yield electrical characteristics [6, 17, 36], and require a relatively large phase change material surface hence are only suitable for thin film

characterization. The micro-stage approaches are faster than conventional slow *R-T* measurements but still too slow to capture the metastable phases at elevated temperatures [3, 37-41]. Also, in device form, four-point electrical measurements are ideal for eliminating contact resistances, however the two contacts made for the voltage measurements introduce significant capacitance to the system limiting the measurement speed and distort the programming pulses [42].

With regard to instrumentation needs for the device characterization, highly resistive amorphous phase of these materials (~MΩs, depending on the device size) and very fast crystallization times (~100 ns close to melting temperature) has to be considered. Parameter analyzers can provide very sensitive DC current-voltage (*I-V*) measurements (< pA), yet they are too slow. Typical oscilloscopes provide a very high resolution in time (~0.2 ns), but the voltage resolution is limited (~1 mV). The DC offsets in oscilloscopes vary over time, making it impossible to get well-calibrated DC measurements in the μV range using an oscilloscope. Additionally, the data depth of oscilloscopes is limited (10 million points in our case); thus, the high-resolution pulse cannot be monitored along with the whole crystallization process using a single oscilloscope. Data acquisition modules can provide practically unlimited recording duration; however relatively lower resolution in time (~10 ms) and voltage (~100 μV).

As a result, highly sensitive, high-speed, two contact device characterization technique is desirable to characterize the PCM materials in a wide temperature range (300~1000 K). This requires an effort on advanced characterization of material systems and device concepts with new approaches.

1.2 Impact of material parameters in phase change memory devices

The present day challenges are to produce PCM devices at smaller scales and reduced power requirements with increased endurance and reliability, which can be realized by well characterized material properties in a wide temperature range in conjunction with accurate modeling of PCM devices with modifications to the existing electron-device models that assume thermal equilibrium, mild temperature variations, and stable material properties [43-49]. In the following sections a few examples of the impact of varying material parameters in PCM device modeling are presented. The temperature dependent material parameters used in modeling studies are presented in Figure 1.3.

Electrical resistivity (ρ) and thermal conductivity (κ) values of TiN are obtained from Gottlieb et al. [50] and Shackelford et al. [51] respectively (Figure 1.3a). Although these parameters are defined as functions of temperature, TiN contacts do not reach as high temperatures as that of the GST bridges; hence this temperature dependence is not critical for the simulations. Heat capacity and Seebeck coefficient of TiN are assumed to have constant values of 784 J/kg.K and 1 μV/K. [46, 49].

Thermal boundary conductivities (TBC) are defined between GST-TiN and TiN-SiO_2 interfaces by adding 1 nm thick virtual layers at the boundaries. Thermal boundary resistance (TBR) at GST-TiN interface is ~20 m^2K/GW between 300 K and 600 K and it decreases significantly when the phase change material melts as it is expected to show a metallic behavior. Hence the TBC is extrapolated to increase up to melting and it is matched to the GST thermal conductivity value at melting temperature. TBC between TiN and SiO_2 is assumed to be constant: 0.05 W/(m.K) (Figure 1.3b) [52, 53].

Temperature dependent electrical resistivity of amorphous GST is measured between 300 K and 675 K and interpolated to the melting point and crystalline (fcc) GST is measured between 550 K and 675 K and interpolated to 300 K with exponential extrapolation assuming no phase transitions [19-24]. Liquid-GST resistivity values used in the simulations is from the experimental results by Endo et al.[54], Kato et al [55], and Cil et al. [56] (Figure 1.3c).

Room-temperature values of the thermal conductivity (κ) of GST as obtained from the literature are considered to be purely due to phonon conduction [53, 57-59]. This term is assumed to be decreasing linearly with GST resistivity, whereas the electronic contribution is calculated to be increasing with temperature following the Wiedemann-Franz law which relates the thermal conductivity and the electrical conductivity of a metal. Total thermal conductivity is calculated as sum of the phonon and electronic components. Thermal conductivity of liquid GST is assumed to be dominated by the electronic conduction due to the large electrical conductivity (Figure 1.3d); contributions from convection in liquid phase are not accounted for [21].

The heat capacity (C_P) of GST is obtained from both Yin et al. [46] and Liu et al. [49] as a constant value of 202 J/(kg.K). Latent heat of fusion of GST is accounted for by a 10 K spike in the heat capacity function for the heat required for solid to liquid phase-change. A 10 K phase-change range is preferred for ease of simulations, instead of a more sudden transition (Figure 1.3e).

Seebeck coefficient (S) of fcc and hcp GST values are measured by Lhacene Adnane up to 740 K in our laboratory. S is extrapolated to be constant between 740 K and

melting temperature (873 K) and assumed to have a small constant value of 1 μV/K in the liquid phase (Figure 1.3f) [60].

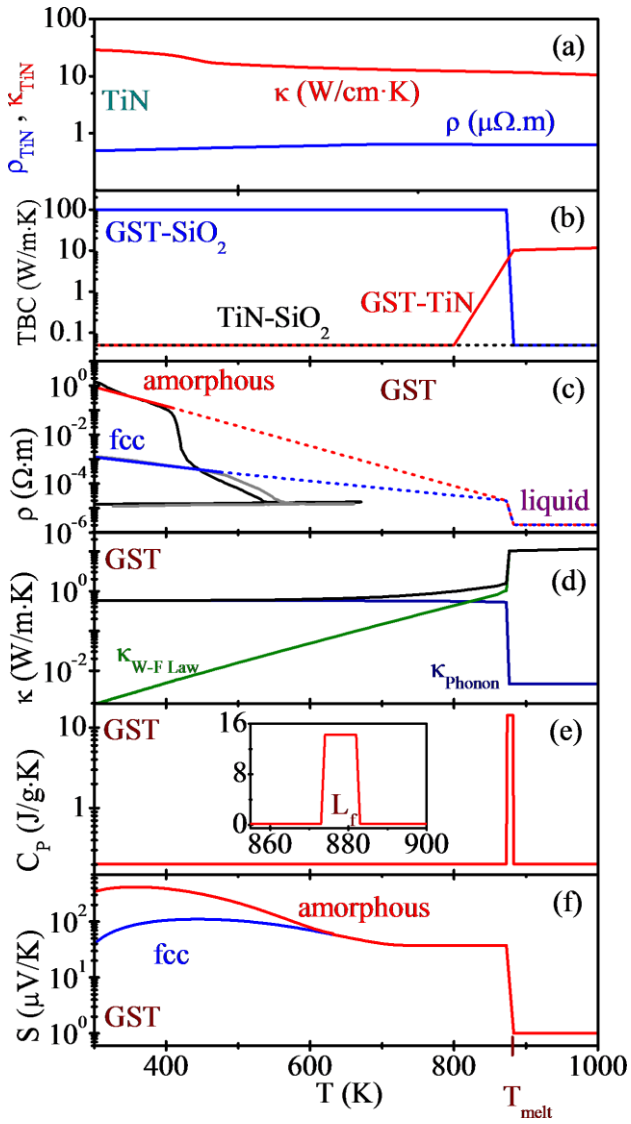


Figure 1.3. Temperature dependent electrical and thermal conductivities of TiN (a), thermal boundary conductivities between GST-SiO_2, GST-TiN and TiN-SiO_2 (b), electrical resistivities of amorphous and fcc GST (c), thermal conductivity of GST (calculated electronic and estimated phonon contributions) (d), Heat capacity of GST around the melting temperature (e), inset showing the peak to incorporate the latent heat of fusion, and Seebeck coefficient of amorphous and fcc GST (f) [19-22, 25].

1.2.1 Liquid GST resistivity

PCM devices experience a large range of operation temperatures (~300-1000 K) and thermal gradients (~10-100 K/nm) while switching between crystalline, liquid, and amorphous phases. Amorphization is achieved by using a large-amplitude short-duration electrical pulse which melts small volume of a phase change material and allows it to quench. Crystallization is obtained by either using a small-amplitude and long-duration pulse which heats the amorphized region just above the crystallization temperature ($T_{cryst\text{-}GST}$ ~425 K) for a sufficient time or melting followed by slowly cooling. Melting is required for amorphization (and crystallization), thus liquid material properties has to be well defined. Even though GST is the most studied phase-change material, only two experimental values for electrical resistivity of liquid GST were reported: ~0.4 mΩ.cm based on bulk GST measurements and ~4 mΩ.cm based on film measurements. This ~10x disparity is very significant for device modeling (Figure 1.4) [19-22, 54-56, 61]. The impact of liquid GST resistivity is illustrated by numerical simulations performed using COMSOL multiphysics (Figure 1.4).

Two experimental values for liquid GST resistivity obtained from literature are used to model a typical- mushroom type PCM device shown in Figure 1.4 with 2D rotational symmetry for reset operation [56]. Simulations resulted in distinctly different temperature profiles and operation dynamics between two different liquid GST resistivity values. Simulation performed using a higher resistivity value show a filament formation before forming a mushroom shape amorphized region. As a result, well characterized liquid GST resistivity is required for complete modeling.

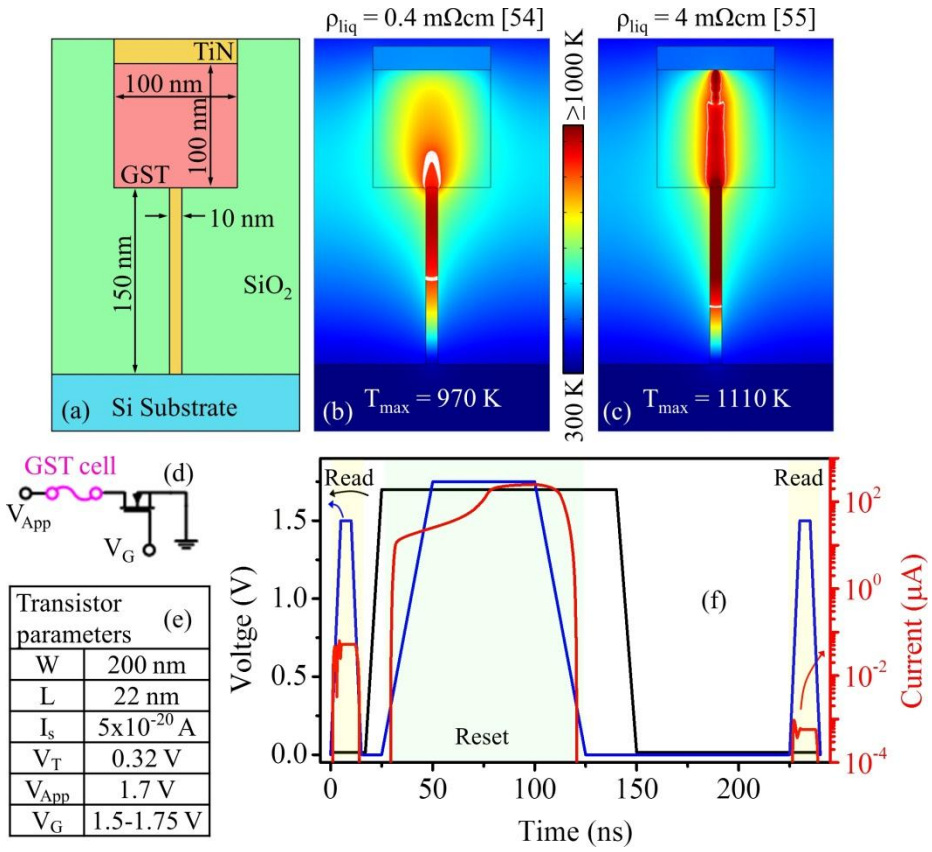


Figure 1.4. Simulated mushroom type PCM device using previously reported experimental values for the electrical resistivity of liquid GST [54, 55] and temperature profiles at 100 ns. The white contour lines indicate the solid-liquid transition temperature range (assumed as 873 K-883 K), within GST (a-c). Schematic illustration of modeled circuit (d). Access transistor parameters used in the model (e). Sample simulation results: applied voltages and obtained current through a GST structure (f).

1.2.2 Metastable GST resistivity

The electrical resistivity of the device changes by orders of magnitude (~10-10^4 times depending on the active region size) as a function of temperature while it is switching between amorphous and crystalline phases. Understanding of this temperature dependency is crucial for realistic modeling of PCM device operation. Electrical resistivity of GST has been reported as a function of temperature based on typical slow

resistance versus temperature (*R-T*) measurements (typical ramp rate of ~1 K/min) [2, 3, 62, 63]. However PCM devices operate in the order of nanoseconds and the PCM materials are expected to retain a metastable phase until melting during reset and set operations. Therefore, significant differences are expected between the simulations, using *R-T* values based on slow measurements and more realistic metastable material characteristics [19-25].

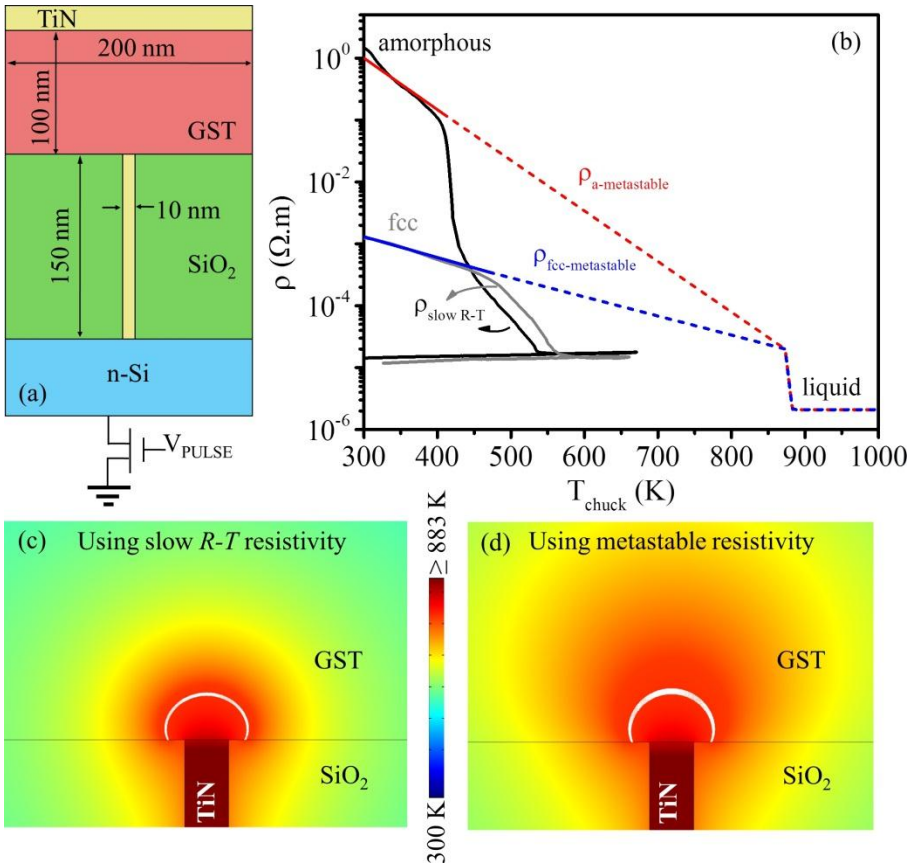


Figure 1.5. Schematic illustration of mushroom type PCM cell used for simulations (a). Electrical resistivity based on slow *R-T* measurements and metastable resistivities based on exponential extrapolation (b). Temperature profiles of simulated structures at the end of 100 ns amorphization (reset) pulse using *R-T* values based on slow measurements (c) and metastable extrapolations (d) (Simulations are performed by Azer Faraclas).

The difference in device operation dynamics has been demonstrated through simulation of a mushroom type PCM cell with 2D rotational symmetry for reset operation using COMSOL Multiphysics (Figure 1.5a) [22]. Here, metastable resistivity functions were generated by extrapolating the slow *R-T* measurement results between 300 K and 873 K exponentially (Figure 1.5b). Simulations resulted in distinctly different temperature profiles even though the molten region volumes are comparable (Figure 1.5c,d). Also, metastable model showed a filament formation before forming mushroom shape amorphized region for a fast (1 ns) rise-time (Figure 1.6). Results show that well characterized, more realistic metastable amorphous and fcc GST resistivity values are required for complete modeling.

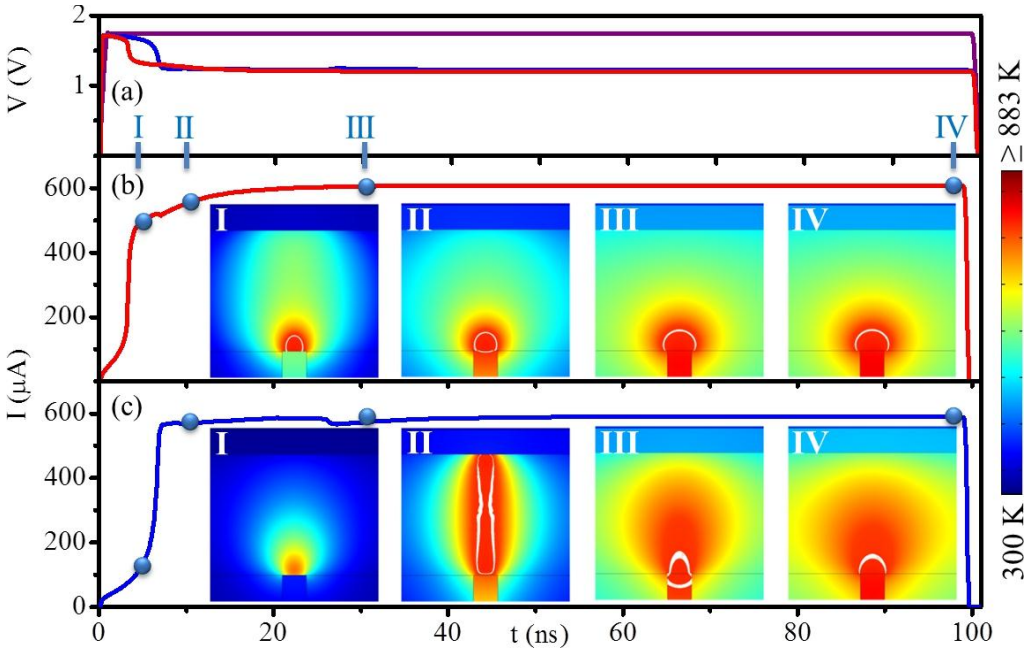


Figure 1.6. Applied voltage and voltage across the cell (a), current through the cell for slow *R-T* resistivity (b) and metastable resistivity (c) models. Insets are the temperature profiles of simulated structures at various time steps during the reset operation (Simulations are performed by Azer Faraclas).

1.2.3 Thermoelectric effects in phase change memory devices

Switching of PCM devices are achieved by a suitable electrical pulse leading joule heating which is the heat generated when an electrical current is passed through a conductor, also known as resistive heating. In addition to this, thermoelectric effects also play significant role in heating. These effects are the result of energy/heat carried by generation, transport and recombination of charged carriers [64], namely: i) Seebeck effect: Voltage build-up across a temperature difference $(S = dV / dT)$, ii) Peltier effect: Heat transfer by charge carrier flow across a junction of two different materials $(\Pi = ST)$, iii) Thomson effect: Heat transfer by charge carrier flow along a uniform material due to a temperature gradient $(\beta = T(dS / dT))$.

Joule heating (J^2 / ρ) on a uniform and symmetric structure is expected to result in a symmetric temperature profile. However, the number of carriers and their energy changes along the temperature gradient on the structure. Generation processes absorb energy while recombination events release. Transport of the charged carriers can lead to a significant disturbance in generation-recombination balance and result in drastically asymmetric self-heating at elevated temperatures. At lower temperatures the thermoelectric transport is dominated by electronic-convective heat flow. Both of these processes lead to thermoelectric heat transport in single material systems known as Thomson heat: $-T(dS / dT)J \cdot \nabla T$ where, S is the Seebeck coefficient. The skew direction of the temperature profiles due to Thomson effect depends on the dominant mechanism, which is manifested as changes in Seebeck coefficient with temperature. $|dS / dT|$ increases with temperature if electronic-convective process is dominant.

$|dS/dT|$ decreases with temperature as thermally generated carrier concentration become significant and the material starts turning intrinsic [64, 65].

Experimental observations of thermoelectric effects have been previously reported for *p*-type polycrystalline silicon (poly-Si) micro-lamps, *n*-type poly-Si micro heaters and micro-bridges through asymmetric self-heating and light emission [64-68]. It has also been reported that thermoelectric effects on PCM cells result in asymmetric self-heating and amorphization [19-21, 31, 32, 69-74]. Hence, thermoelectric effects must be taken into account during the modeling and design of these structures.

As part of this research effort, 3D modeling of thermoelectric effects is performed on GST bridge structures using COMSOL Multiphysics to get insight about the relative contributions in various geometries. The GST bridge structures are suspended and anchored on large Titanium nitride (TiN) contacts with varying 3D geometries (line, dog bone, T, and wedge) for the modeling as seen in Figure 1.7. Crystalline to amorphous phase change (reset) is modeled assuming that any molten region becomes amorphous at the end of the voltage pulse. An access transistor using a SPICE model is integrated with the finite element simulations in COMSOL. Initial (set) and final (reset) resistances are extracted using small read signals before and after the reset pulse.

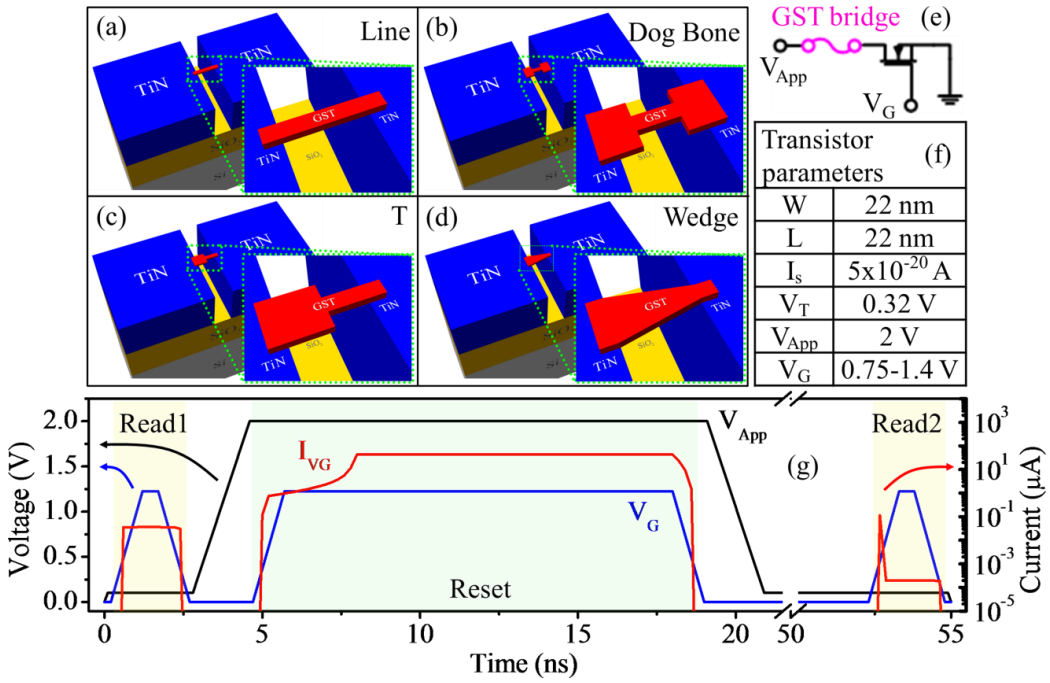


Figure 1.7. 3D view of the simulated structures with thicknesses of 10 nm (GST), 250 nm (TiN), 250 nm (SiO_2) and 500 nm (Si). TiN contacts are 500x500 nm^2 square. The gap between the TiN contacts is 100 nm. The GST bridge overlaps 20nm into each TiN contact (a-d). Schematic illustration of modeled circuit (e). Access transistor parameters used in the model (f). Sample simulation results: applied voltages and obtained current through a GST structure (g).

The model simultaneously solves electrical conduction (Equation 1.1) and heat transfer (Equation 1.2) equations to find the temperature and voltage on the structure while applying a nanosecond voltage pulse on the TiN contact pads. Current continuity is assumed for the electrical conduction. The thermoelectric heat is included in Equation 1.2 as a heat source which is the Peltier heat at a junction and Thomson heat in a uniform material:

$$\nabla \cdot J = \nabla \cdot (-\nabla V - S\nabla T)/\rho = 0 \tag{1.1}$$

$$d\,C_P\,dT/dt - \nabla \cdot (k\nabla T) = E \cdot J - J \cdot \nabla(ST) \tag{1.2}$$

where, ρ is the electrical resistivity, S is the Seebeck coefficient, d is the mass density, C_P is the heat capacity, E is the electric field, and k is the thermal conductivity.

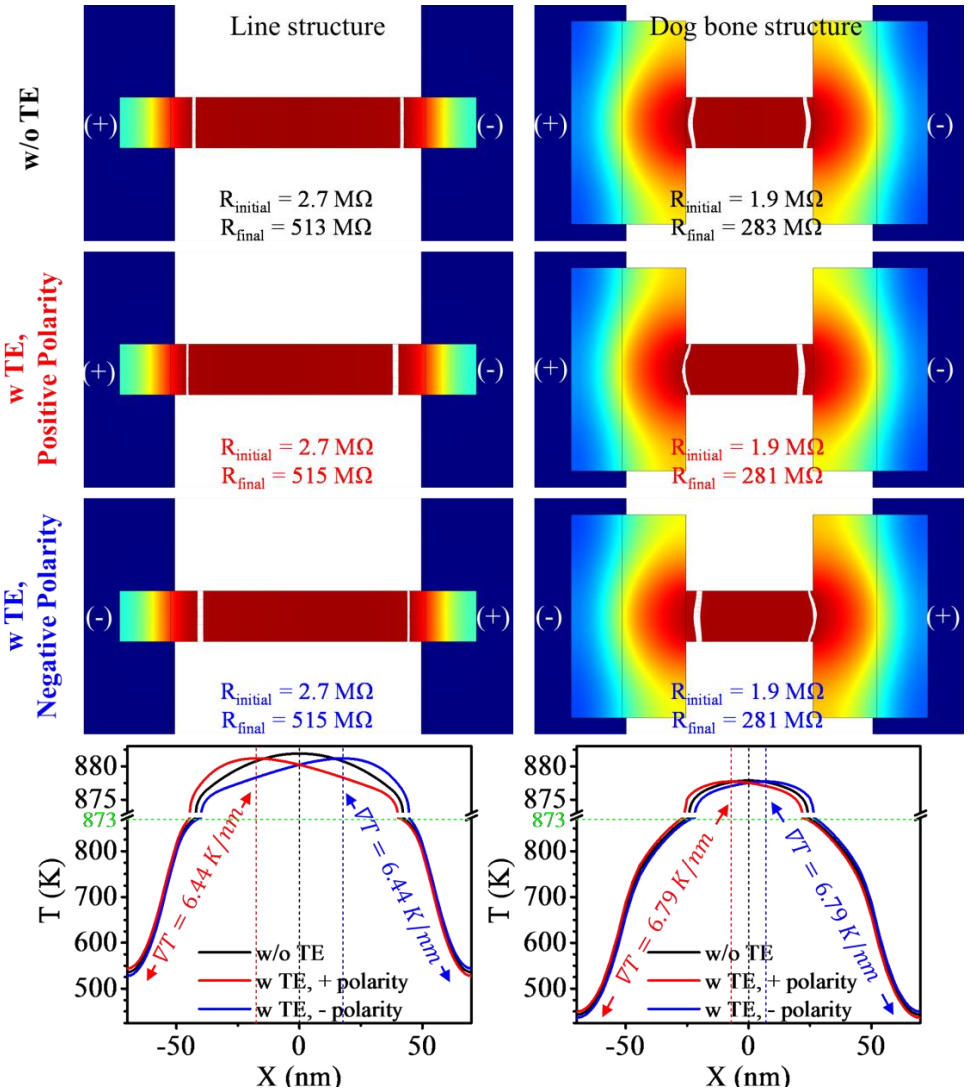


Figure 1.8. Temperature profiles across the symmetric line (left) and dog bone (right) bridge structures during the pulse (t: 18 ns, I: 43μA). White contour lines indicate molten regions (T > 873 K). Vertical dashed lines in bottom plots indicate the peak temperature locations without TE (black), with TE and positive polarity (red), and with TE and negative polarity (blue) cases. The scale is expanded for T > 873 K to highlight the details beyond onset of melting.

When thermoelectric effects are not included in the model, the bridge cells heat up symmetrically and start melting at the center as expected. With the inclusion of the thermoelectric terms, the hottest spot on the bridge skews towards the higher potential end prior to melting. The white contour lines (T = 873 K) mark to the extent of the molten region (Figure 1.8). Current through the bridge is limited by the access transistor which is controlled by the gate voltage. Figure 1.9 shows the resistance contrast between reset and set states for the cases without and with thermoelectric effects (TE) while varying the gate voltage, hence the GST bridge current. Room temperature reset resistance is calculated assuming that any mesh point that experiences 873 K is amorphized upon resolidification. The reset resistance is ~150-200 times larger than the set resistance for the highest current levels. The simulation results show that TE does not impact the cell resistance in symmetric structures as it does not matter which part of the bridge is amorphized.

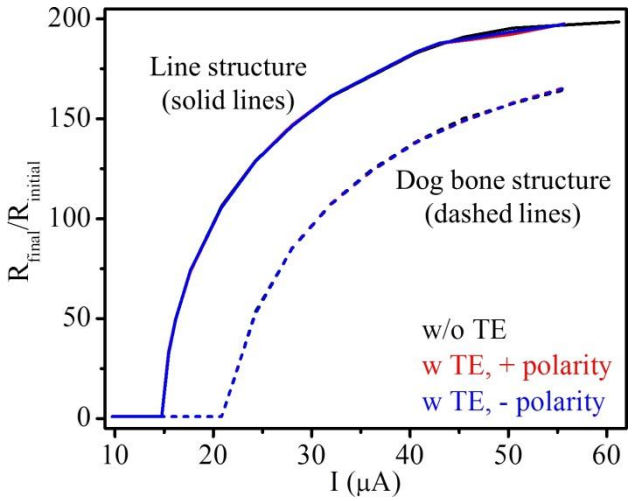


Figure 1.9. R_{reset}/R_{set} ratio for symmetric line (solid lines), and dog bone (dashed lines) bridge structures.

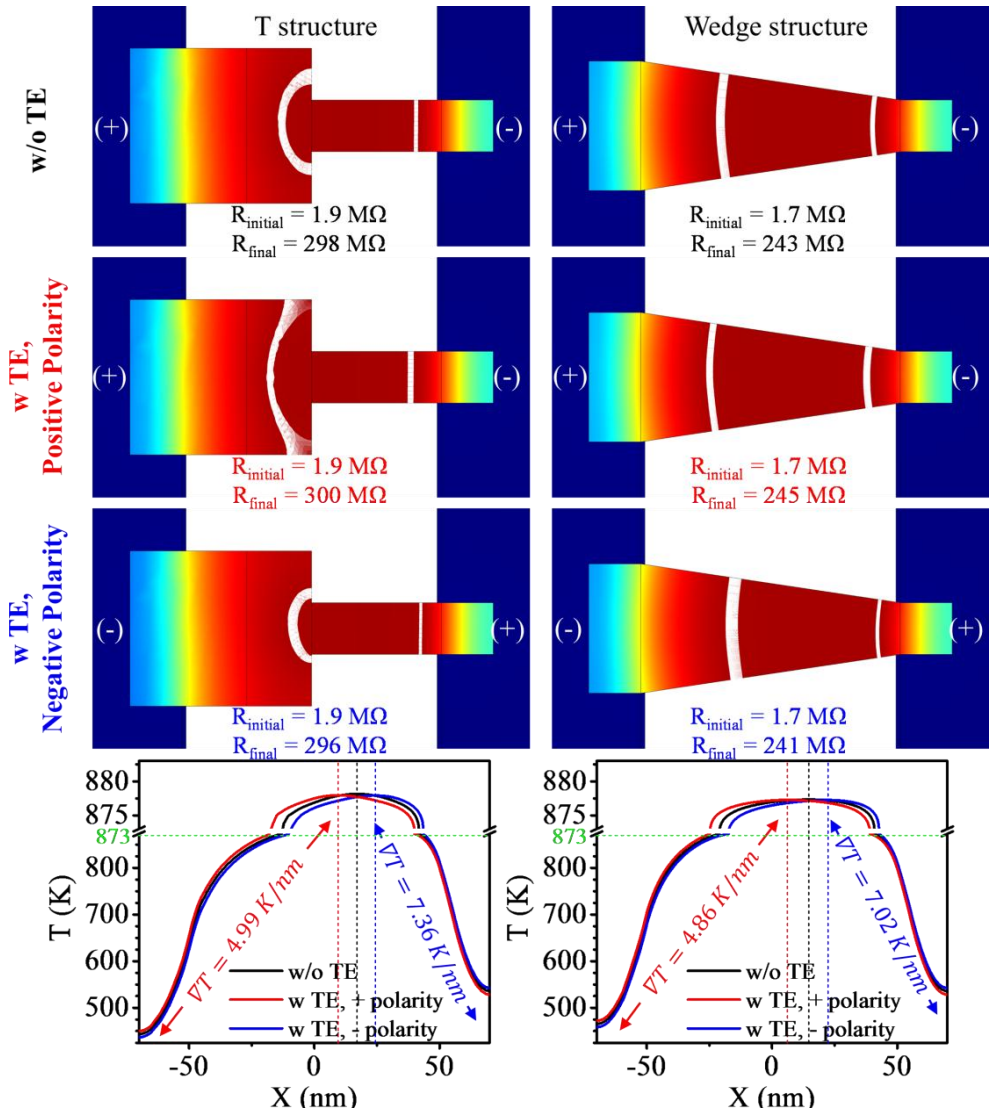


Figure 1.10. Temperature profiles across the asymmetric T (left) and wedge (right) bridge structures during the pulse (*t*: 18 ns, *I*: 43μA). White contour lines indicate molten regions ($T > 873$ K). Vertical dashed lines in bottom plots indicate the peak temperature locations without TE (black), with TE and positive polarity (red), and with TE and negative polarity (blue) cases. The scale is expanded for $T > 873$ K to highlight the details beyond onset of melting.

Simulated temperature profiles on asymmetric T-shape and wedge shape bridge structures (Figure 1.10) show that the reset/set resistance ratio is larger for the positive polarity (181), compared to the negative polarity (171) and without TE cases (175) in

asymmetric T structures. The wedge structure shows similar results: (R_{reset}/R_{set}: 175 for positive polarity, 160 for negative polarity, and 168 for without TE) (Figure 1.11). The contribution of the TE effects increases with increasing current density. These simulation results are in-line with reports that show reduced power requirements for reset operation on asymmetric structures with the preferred polarity [19-22, 31, 32, 71-74]. Furthermore, the temperature gradients can be significantly different for the two polarities which can result in reliable operation in one voltage polarity and rapid failure in the opposite polarity as reported in [73, 74]. This may be due to accelerated elemental segregation in one polarity due to larger thermal gradients (Figure 1.8).

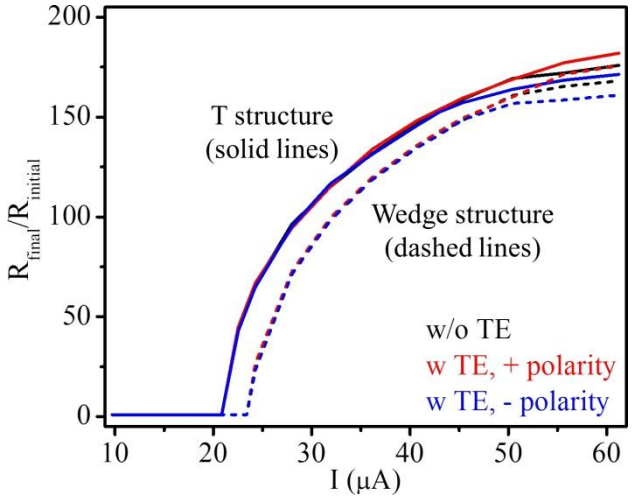


Figure 1.11. R_{reset}/R_{set} ratio for asymmetric T (solid lines), and wedge (dashed lines) bridge structures.

More heating on the higher potential end of the bridge is due to heat released by the charge carrier on this side as their Peltier coefficient decreases with increasing temperature. On the other side of the bridge, however, the carriers absorb energy due to their increasing average energy, leading to less heating on this side. This asymmetric heating on the bridge results in the shift in the hottest spot towards the higher potential

end side before the bridge starts melting. Thermoelectric effects do not affect the reset/set resistance contrast on the symmetric structures (Figure 1.9), although the resulting asymmetric amorphization will cause subsequent programming steps to be polarity dependent. The skewed temperature profiles also result in larger temperature gradients on one side of the bridge (Figure 1.8) which may exacerbate the segregation of elements in GST, hence accelerate the device failure.

The overall impact of thermoelectric effects is minimal for lateral structures that have contacts away from the active area. In these devices melting profile is not as important, since any molten/amorphized section has a similar impact on R_{reset}/R_{set} ratio. Thermoelectric effects have more profound impact on operation dynamics of mushroom cells which have their active region in contact with one of the electrodes and current spread is very significant [19].

This work focuses on experimental characterization of temperature dependent metastable materials characteristics, crystallization dynamics and resistance drift, all of which are critical for PCM design. A highly sensitive, high-speed technique has been developed to characterize phase change materials at nanoscale device level at high temperatures.

2. Fabrication of phase change memory devices

Nanoscale lateral PCM device structures are easier to fabricate with better dimension control. Additionally, a large variety of device dimensions and geometries can be fabricated on the same wafer using conventional fabrication techniques. Hence, the experiments were designed to use lateral structures instead of vertical structures to investigate electrical, thermal and electrothermal material properties. A sub-set of these devices are used for high temperature and high speed material characterization, crystallization dynamics and resistance drift phenomena in device level as described in Chapter 3. The devices used in this study were fabricated at IBM T. J. Watson Research Center and characterized at the University of Connecticut under a joint study agreement.

2.1 Layout design

Two levels (RX: active level and M1: metal level) of optical lithography is used for fabrication of PCM devices used in this work. Layout design of the PCM devices used here has two generations. First generation layout design (done by Mustafa Akbulut) has devices ranging from 180 to 540 nm in length (L) and from 80 to 720 nm in width (W). 20nm and 50 nm thick (t) devices on Silicon dioxide (SiO_2) substrate are fabricated using this design. This mask set is redesigned using Layout Editor [75] by fixing the bugs in the first generation layout design, optimizing device dimensions (*L:* 180 nm to 91 µm, *W:* 80 to 720 nm) and adding new test structures such as staggered device arrays for cross section imaging, film thickness measurement sites, large probing devices. 20nm, 50 nm,

and 100 nm thick (*t*) devices on SiO_2 (some samples on Silicon nitride (Si_3N_4)/SiO_2 stack) substrates are fabricated using this design. Layout of the fabricated structures is shown in Figure 2.1 with various magnifications.

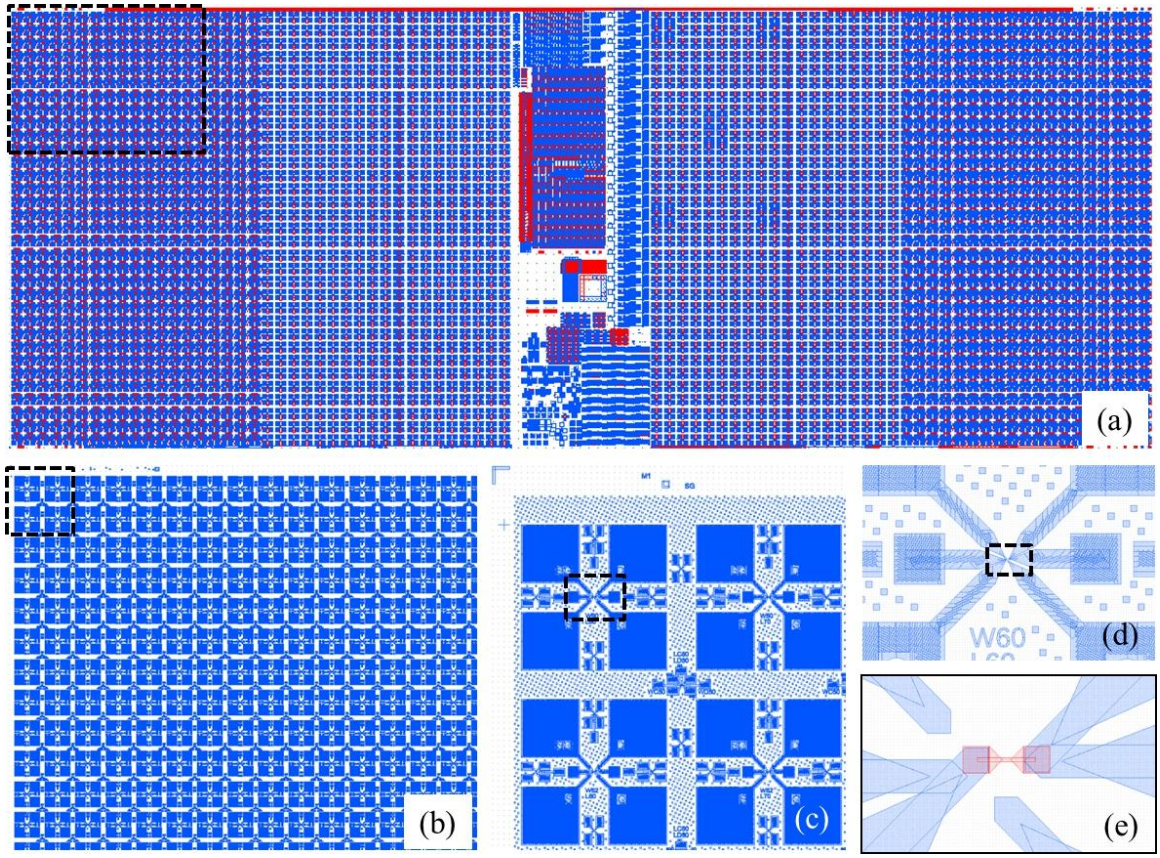


Figure 2.1. View of the die and a sample device (W: 60 nm, L: 60 nm) with various magnifications. Device arrays with dimensions ranging from 180 to 540 nm in length (*L*) and from 80 to 720 nm in width (*W*) as are located in left and right side of the die and other test structures (detailed in Appendix 5.1) are located in the middle. Die size is 2.6 cm by 1.0 cm and 97 full dies are located on an 8 inches wafer.

6 levels of mask are printed on two reticles based on the critical dimensions of device features. The process uses 193 nm wavelength optical lithography employing reticles printed on 6x6x0.250 inches quartz substrate with 4x magnification compatible to the ASML PAS5500/1100 (193 nm) stepper tool at IBM T. J. Watson Research Center.

The details of the layout and mask design are presented in Appendix 5.1 and Appendix 5.2.

2.2 Device fabrication

Fabrication process consists of two levels of 193 nm wavelength optical lithography with critical dimension of 60 nm for the active level (GST line cells) and 300 nm for the metal level. GST needs to be capped with a diffusion barrier to prevent oxidation and evaporation. This capping layer also prevents reaction of GST with solvents in photoresists as well as acetone, making it difficult to use typical metal lift-off processes to form contacts. GST is deposited using low temperature processes compatible with underlying metal layers. Hence, bottom contacts were preferred for the experiments in this study. TiN and tungsten (W) (commonly used metals for PCM) were preferred as their thermal conductivities are lower than other common alternatives such as aluminum or copper. The GST device integrity is better preserved if the bottom contacts do not have a step height compared to the surrounding dielectric material. A Damascene process [76] is used to form the bottom contacts without a step height.

The GST line cells used in these experiments are fabricated as follows: 600 nm SiO_2 is thermally grown on Silicon (Si) wafers (100 nm Si_3N_4 is deposited on 600 nm SiO_2 using LPCVD system on some samples) (Figure 2.2a) and 250 nm deep trenches are etched into the SiO_2 layer (100 nm into Si_3N_4 and 150 nm trenches into SiO_2 for samples with Si_3N_4/SiO_2 stack) using optical lithography and reactive ion etching (RIE) (Figure 2.2b). The trenches are filled with a 300 nm thick TiN using chemical vapor deposition (CVD) and physical vapor deposition (PVD) systems (some samples with W using CVD

system) (Figure 2.2c). The wafers are then polished using chemical and mechanical planarization (CMP) to form planar bottom contacts (Figure 2.2d). Undoped GST films (thickness of 20, 50, 100 nm) are deposited by co-sputtering from elemental targets at room temperature (amorphous phase), followed by sputter deposition of a 10 nm SiO_2 cap layer (Figure 2.2e). The GST line cells are then patterned using optical lithography and RIE. A 15 nm thick Si_3N_4 (SiO_2 for some samples) blanket encapsulation layer is then deposited by plasma-enhanced chemical vapor deposition (PECVD) protecting the devices from oxidation and evaporation (Figure 2.2f,g). The final device dimensions are determined using a scanning electron microscope (SEM). The details of the fabrication process and a list of fabricated structures are provided in Appendix 5.3.

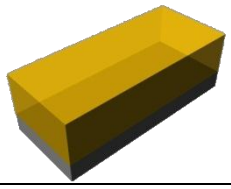
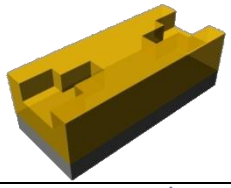
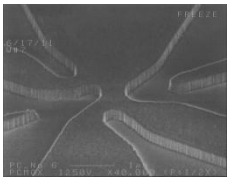
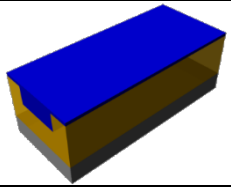
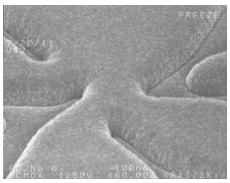
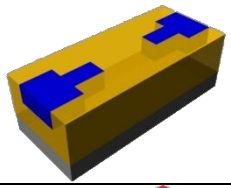
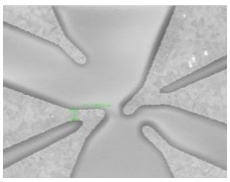
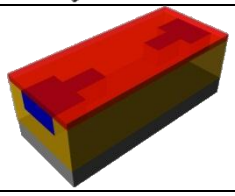
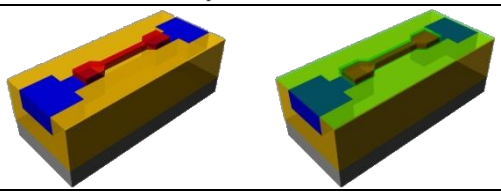
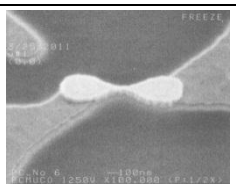
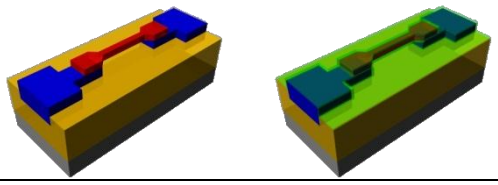
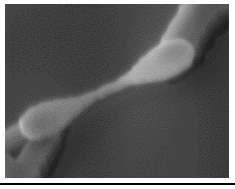
	Schematic illustration	SEM image	Process description
a		-	600nm SiO_2 growth on Si substrate
b			250 nm deep trench formation into SiO_2
c			300 nm TiN (or W) metal deposition
d			Chemical mechanical planarization (CMP)
e		-	GST film deposition
f			Patterning GST line cells and capping with Si_3N_4 (or SiO_2) layer
g			Suspending GST line cells and capping with Si_3N_4 (or SiO_2) layer

Figure 2.2. Schematic illustrations of the GST line cell fabrication process steps and corresponding SEM images of fabricated structures.

2.3 Devices used for experiments

Measurements presented here are from 2-point measurements performed on a large number of GST line cells with varying dimensions (minimum feature size is ~100 nm) (Figure 2.3), fabricated as depicted in Figure 2.2.

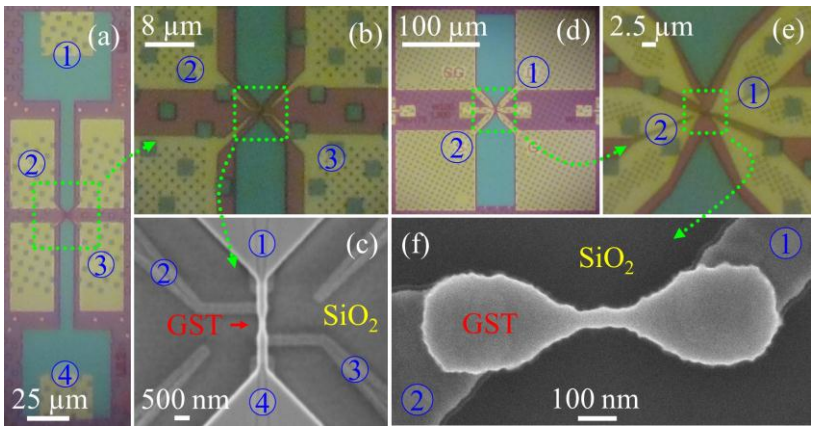


Figure 2.3. Optical microscope (a, b, d, e) and SEM (c, f) images of 4 contact (a, b, c) and two contact (d, e, f) devices.

The metal-GST contacts are characterized to be close to ideal ohmic contacts based on 4-point and 2-point measurements performed on test structures shown in Figure 2.4. Comparison between 2-point and 4-point measurements shows that there are no significant contact resistances on GST line cells. Also, there is no significant difference between devices with TiN and W contact Figure 2.4.

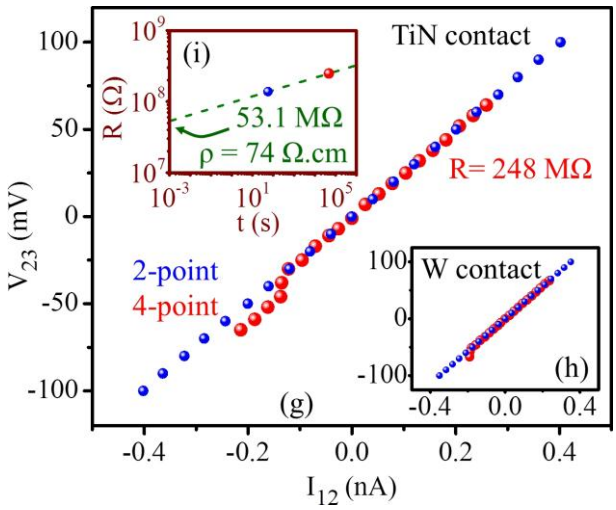


Figure 2.4. *I-V* characteristics using 4-point (red) and 2-point (blue) DC measurements on devices with TiN contacts (g) and W contacts (h). Resistance and resistivity extraction from extrapolation of DC measurements to 1 ms, to take into account the resistance drift in amorphous phase and to compare results from AC high-speed measurements (i).

Metal extension resistances are characterized on structures shown in Figure 2.5 using DC current-voltage (*I-V*) measurements with Agilent 4156C parameter analyzer (PA) [77] and found as R_M = ~200 Ω at 300 K [56].

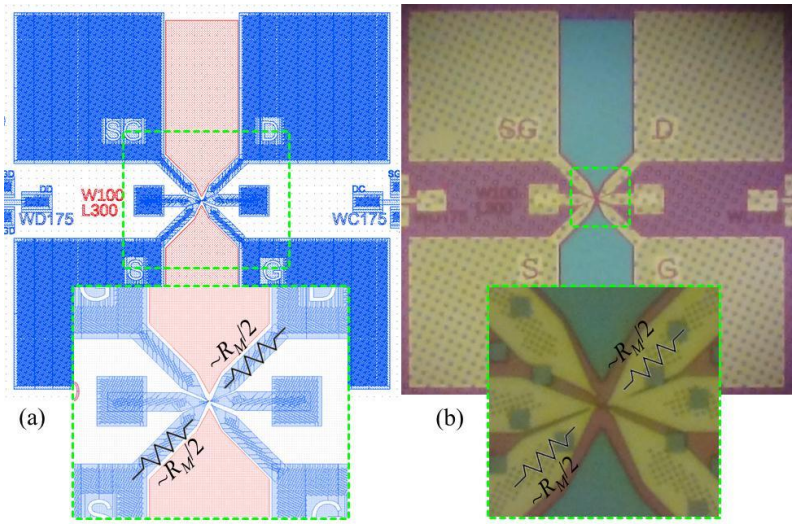


Figure 2.5. Layout (a) and optical microscope images (b) of metal extensions.

Temperature dependent electrical resistivity of TiN contacts is measured using 4-point measurements on big metal resistivity structures located at the bottom of the die illustrated in Figure 2.6 in 300-675 K temperature range.

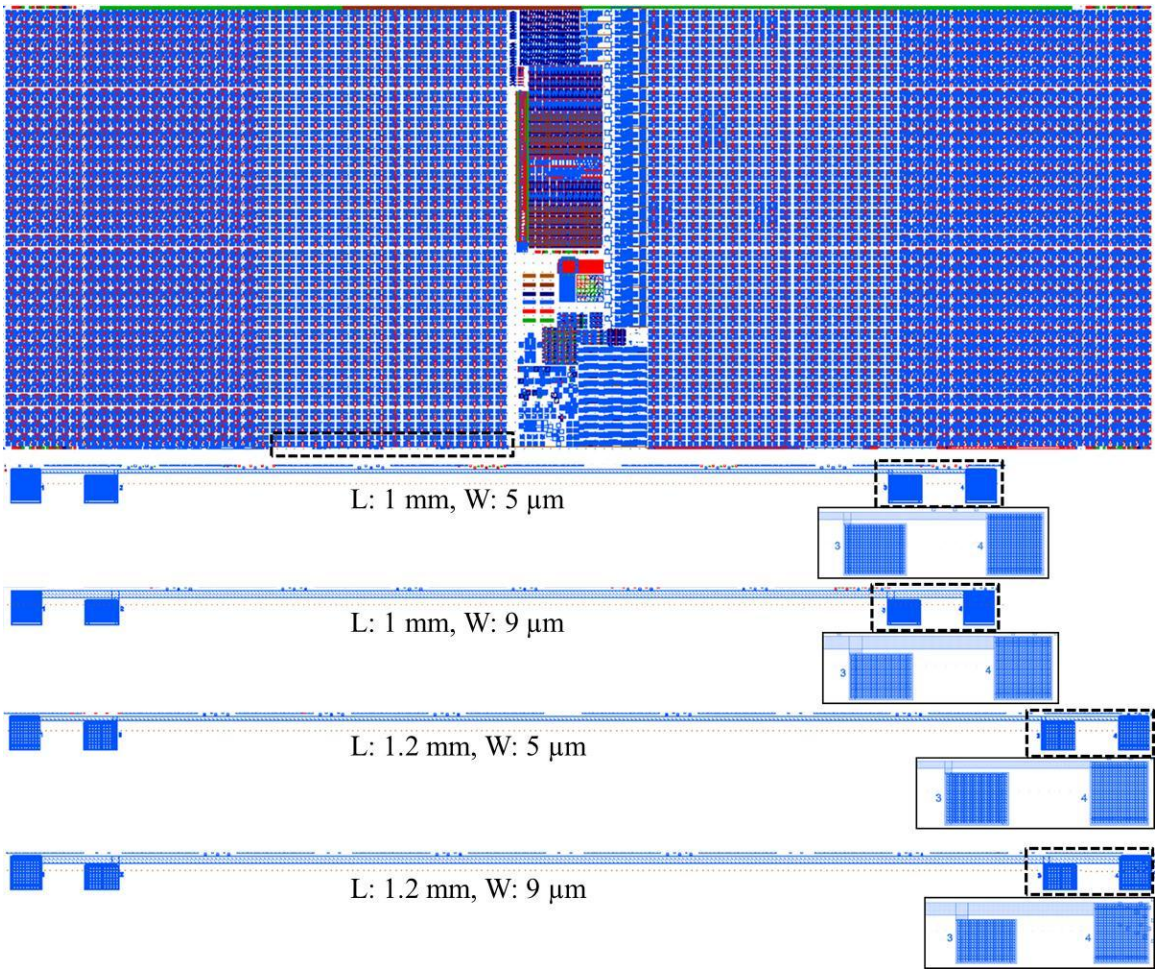


Figure 2.6. Layout of big metal resistivity structures for resistivity measurement.

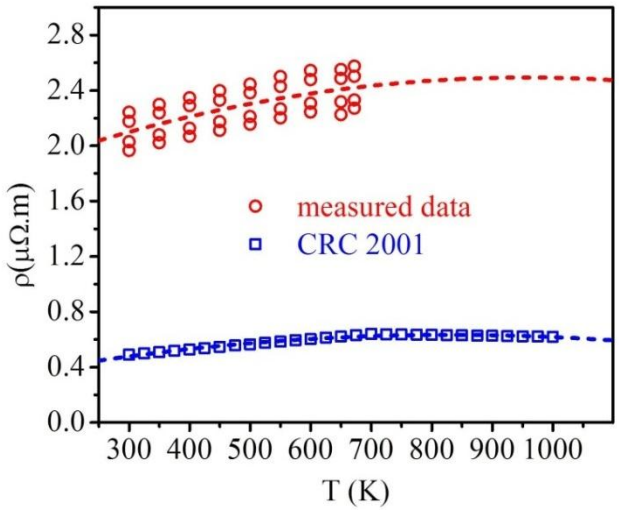


Figure 2.7. Electrical resistivity of TiN as a function of temperature.

The electrical resistivity of TiN used in this work is ~4 times larger compared to reported values in literature [50]. Results obtained from 4 samples and the data obtained from the literature are shown in Figure 2.7.

3. Electrical characterization of GST phase change memory devices

The approach demonstrated in this work is a device-level high-speed electrical characterization technique for phase change materials in a temperature range of 300 K-675 K and it can be used for any phase change material at any temperature range possible for a specific experimental setup [56, 65]. Electrical resistivity of liquid GST is extracted by applying a simple rectangular voltage pulse with 1 μs duration to the line cells at the earlier stage of this work. This technique was further developed to extract more information from a single measurement using a tailored waveform: GST line cells are amorphized by an electrical pulse induced self-heating and the device resistances are monitored before, during and after amorphization for short (~2 ms) and long (~30 min) time durations at various chuck temperatures (T_{chuck}). Using this technique, electrical resistivities of metastable amorphous and crystalline (fcc) phases are extracted for the first time. Liquid and crystalline (fcc and hcp) phase electrical resistivities are also extracted as part of the same measurement. Carrier activation energies are calculated from these results. Short term and long term crystallization and resistance drift behaviors are also monitored as part of the same measurement. In addition to these, electrical breakdown field of amorphous GST is extracted using the same approach using a slightly modified waveform. Transport properties such as carrier density and carrier mobility properties of GST are extracted using Hall measurement technique. Memory operation is demonstrated through cycling of these devices.

3.1 Electrical resistivity of liquid GST

Liquid GST resistivity measurements are performed using a set of GST line cells by melting them via self-heating with 1 µs voltage pulses at 500 K chuck temperature, under high vacuum (10^{-5} torr) in Janis ST-500-UHT variable temperature cryogenic probe station [78]. An Agilent 8114A pulse generator [79] is used to apply a 1 µs pulse and a Tektronix DPO4104 oscilloscope [80] is used to measure the applied voltage (V_A) and current (by measuring voltage across the 50 Ω termination resistor) (Figure 3.1). W probe tips are used to make contact with the TiN.

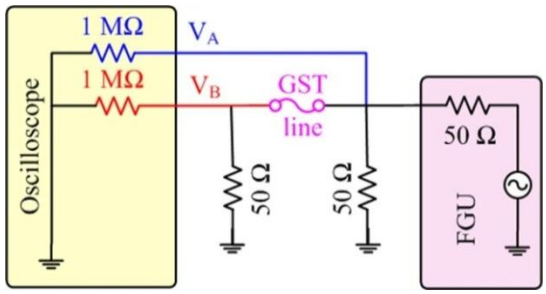


Figure 3.1. Circuit schematic of the experimental setup.

Stable current levels are observed as a plateau once liquid GST path forms, during the pulse indicating complete melting of the structures (Figure 3.2) [81-83].

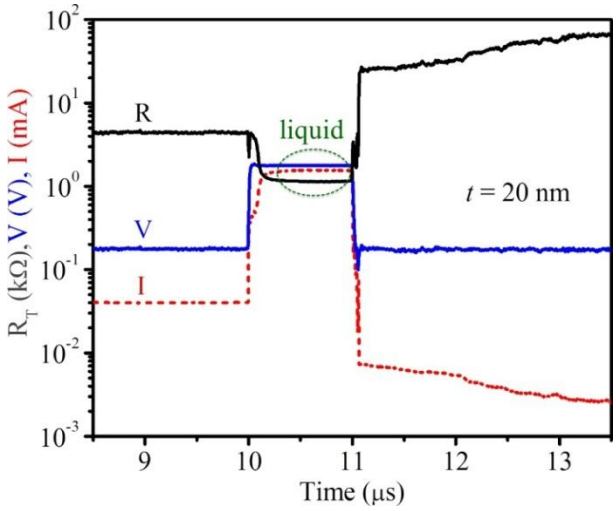


Figure 3.2. Measured voltage (V_A), current (V_B/50 Ω), and total resistance (R_T) as a function of time for an individual device (T = 500 K)

The measured total resistance (R_T) at the plateau includes the GST cell resistance (R_{GST}), metal extension resistance (R_M) (~200 Ω at 300 K) and 50 Ω termination resistance at the scope input. The GST line cell resistance (R_{GST}) includes contact resistance (R_X) at the TiN/GST interfaces.

$$R_T = R_{GST} + R_M + 50\Omega \tag{3.1}$$

$$R_{GST} = \rho \frac{L}{Wt} + R_X \tag{3.2}$$

Total resistance (R_T) is plotted as a function of 1/W for devices with different L. The y intercepts of the linear fits give contact resistance values which are expected to be approximately the same for all devices (R_X = ~100 Ω) (Figure 3.3).

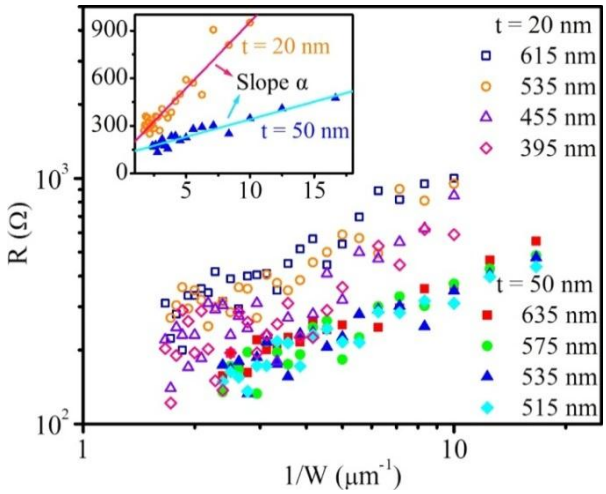


Figure 3.3. R_T during pulse as a function of 1/W of the devices for different length (L) values for two different thicknesses (t: 20 and 50 nm). Inset is the zoomed in version for L = 535 nm and two different thicknesses.

The slopes of these fits ($\alpha = \rho. L/t$) are then plotted as a function of L for two different thicknesses (t: 20 and 50 nm). The slope of these second fits ($\beta = \rho/t$) are used to extract the liquid GST resistivity. The resistivity of liquid GST is measured for the first time in nanoscale device level [56] and extracted as ~0.26 mΩ.cm (Figure 3.4). Previously reported values were ~4 mΩ.cm based on film measurements and ~0.4 mΩ.cm based on bulk GST measurements results [54, 55].

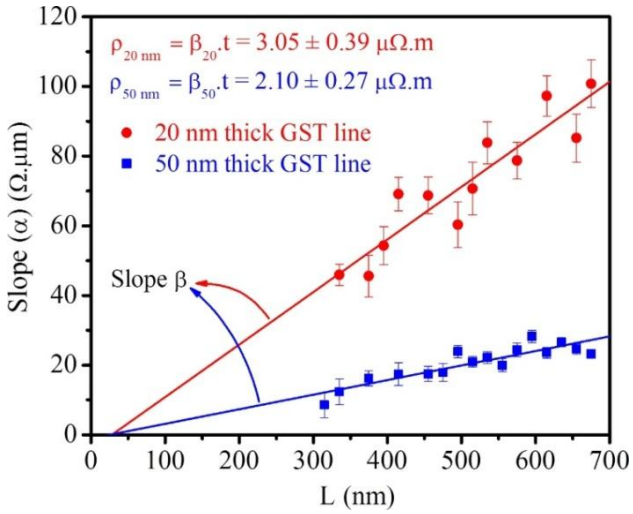


Figure 3.4. Slopes (α) as a function of length (L) and the linear fits for two different thicknesses (t: 20 and 50 nm) [56].

3.2 AC high-speed measurements

We developed a high-speed electrical pump-probe characterization technique to extract temperature dependent resistivity of the metastable amorphous and fcc phases of phase change materials at device level [8, 17, 84-86]. The crystallization process following amorphization and resistance drift in amorphous phase is also electrically monitored for short (~2 ms) and long durations (~3 min to 13 months) as part of the same measurement.

Measurements are performed in a Janis ST-500-UHT variable temperature cryogenic probe station at each temperature point in the 300-675 K temperature range and under high vacuum (10^{-5} torr). Lakeshore 336 cryogenic temperature controller with E-type thermocouple sensor with < 0.5 K resolution is used to control the chuck temperature during the measurements [87]. Tungsten (W) probe tips are used to make contact with the TiN (or W) contact pads. A 1 kΩ current limiting resistor is integrated onto one of the probe tips to introduce a series load with minimal capacitive contributions

and avoid capacitive discharge and relaxation oscillation [81, 83, 88]. A Tektronix AFG3102 function generator unit (FGU) [89] is used and programmed to apply a sequence of electrical signals (1 MHz AC signals before and after a 1 µs pulse and 1 µs cool-down period for a total of 2 ms with a continuous baseline voltage of 50 mV). A Tektronix DPO4104 oscilloscope is used to measure the applied voltage (V_A) and current (by measuring voltage across the 50 Ω termination resistor (V_B) in series with the wire and a 1 kΩ load resistor). A National Instruments NI9219 data acquisition card (DAQ) [90] is used to monitor the baseline voltage and the resulting current on GST line cells for a long period before and after the pulse (~3-30 min) with 100 S/s sampling rate. An Agilent 4156C parameter analyzer (PA) is used to make slow and highly sensitive DC current-voltage (*I*-*V*) measurements. All instruments used for the electrical characterization are controlled by a computer (front panels of control programs developed using Labview are provided in Appendix 5.4). The schematic of the experimental setup is shown in Figure 3.5.

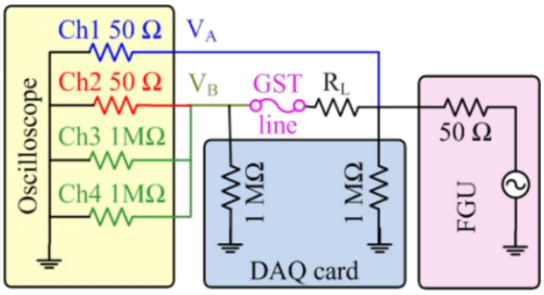


Figure 3.5. Schematic of the experimental setup using a function generator, an oscilloscope and a data acquisition card.

The high-speed electrical measurements are performed using a single-shot waveform containing stepped 1 MHz sinusoidal signal segments with varied amplitudes and a stepped melting pulse (reset pulse) followed by a rapid cool-down for

amorphization (Figure 3.6) [56, 88], in addition to a small DC baseline that is continuously applied to the device (except during the cool-down period following the pulse). A stepped melting pulse is used to extract the liquid phase resistance. The sinusoidal segments are used before and after the pulse to reveal the initial crystalline phase, the metastable amorphous phase resistances, monitor the short-duration crystallization process and resistance drift behavior with high resolution (~2 ms).

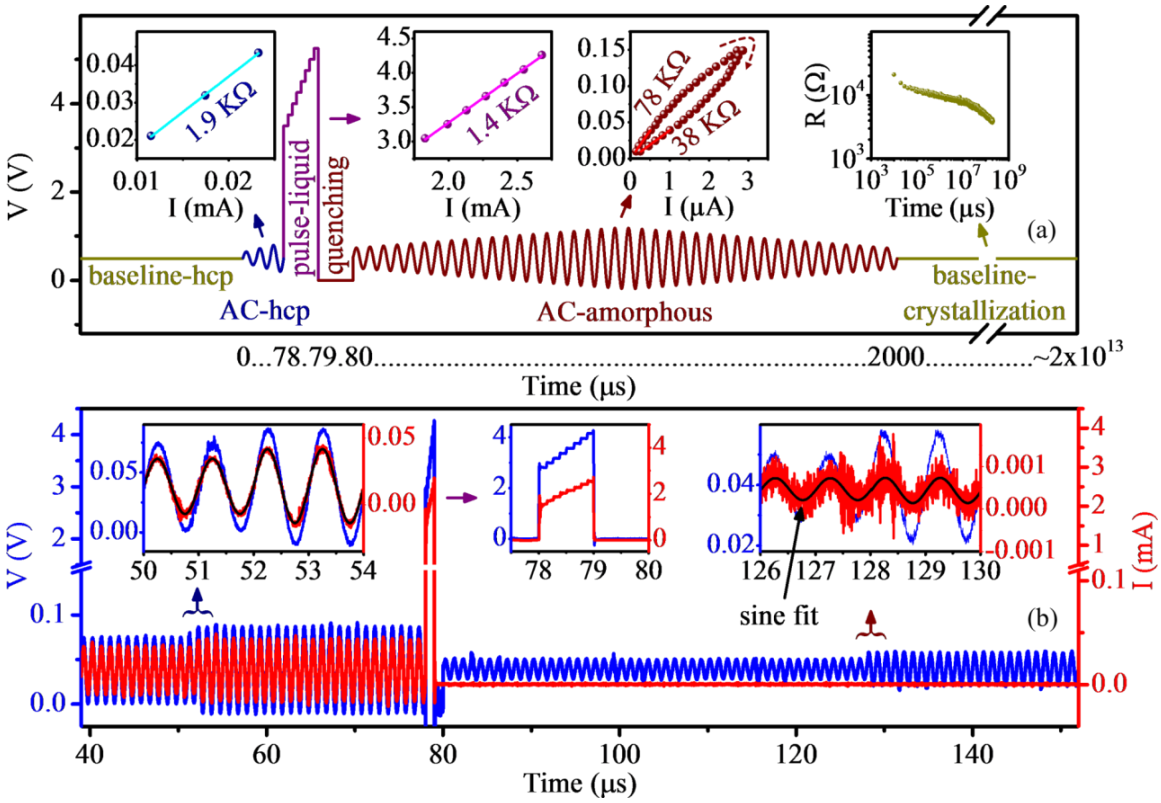


Figure 3.6. Schematic illustration of the measurement waveform, showing the time scales of the each segment. Insets are the *I-V* characteristics obtained from sinusoidal fits before the pulse (0-78 μs), stepped melting pulse (78-79 μs), sinusoidal fits after the pulse (80-2000 μs), and DC baseline measurement showing resistance change in time. Slopes in *I-V* characteristics show total resistances including load, contact, metal extension and GST line cell resistances (a). Example of applied and measured electrical signals showing voltage and current on a GST line cell at 550 K. Insets show zoomed-in view of the signals and sinusoidal fits in crystalline, liquid and amorphous phases (b).

The typical device resistance in the amorphous state is very high -in the order of 40 MΩ- at room temperature; hence the current signal-to-noise ratios are very low. The raw data in each AC segment is fit to a sinusoid with a fixed phase and frequency to extract its amplitude, similar to a lock-in measurement [91]. This AC approach minimizes the random errors due to noise, the problems associated with unknown and varying offset voltages and quantization errors (instrument resolution discrete levels) [92].

The amplitudes calculated from the sinusoidal fits are used to construct the *I-V* characteristics (Figure 3.6 insets) and the resistance values are extracted from the slopes. The amplitude of the AC segments after the pulse are stepped up and then down to check for hysteresis, which would indicate changes in the material during this measurement period (Figure 3.7). The *I-V* characteristics in the liquid state are measured using a melting pulse with small voltage steps that are longer than the transient response associated with charging of the parasitic capacitances. The liquid state resistances extracted from the *I-V* characteristics are used to verify successful melting of the line cells. A 1 μs cool-down period (applying 0 V to the line cells and allowing the cell to return to chuck temperature) is used after the pulse to achieve rapid solidification prior to restoring the DC baseline voltage level with the restart of the AC signal. This eliminates the possibility of retaining a liquid filament after the pulse [93]. Our experimental and modeling results verify that the device temperature returns to the chuck temperature within this 1 μs cool-down period. The DC baseline voltage is used to monitor the recrystallization process for 3 min to 30 min, depending on the measurement temperature, which also verifies the integrity of the structure. A data acquisition (DAQ) card with 10 ms resolution connected in parallel to the oscilloscope is used to acquire the data directly

into the memory of the computer for the long duration measurements providing practically unlimited recording duration. The DC and the sinusoidal signal amplitudes used for the measurements are chosen to be large enough to achieve measurable current levels and yet small enough to not cause significant self-heating (25 nA $\leq I_{wire} \leq$ 5 μA).

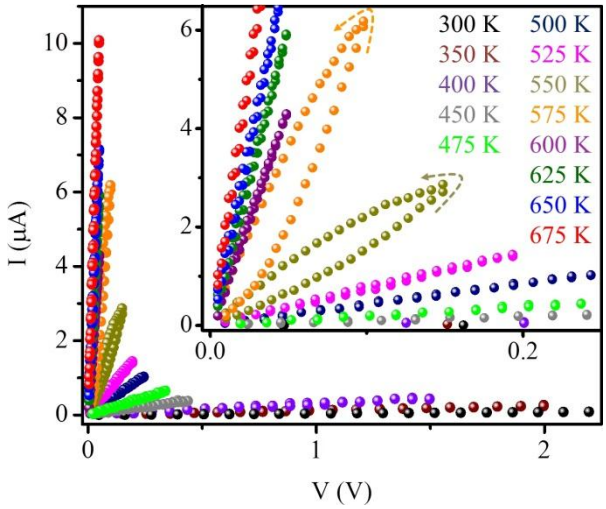


Figure 3.7. Example *I-V* characteristics based on the high-speed measurements. Inset is the zoomed in view highlighting the hysteresis loops seen for T_{chuck} = ~525-600 K measurements.

3.3 Experimental procedure

GST line cells are annealed at 680 K before each set of pulse measurements; hence all of the samples are in the crystalline (hcp) phase for each individual measurement. Electrical measurements consist of 4 main steps: measuring i) initial crystalline (hcp) cell resistances, ii) liquid cell resistances, iii) amorphous cell resistances, and iv) monitoring resistance change over time.

i) Initial crystalline (hcp) cell resistances are measured using three methods:

First, GST line cells resistances are measured using DC current-voltage (*I-V*) measurements by sweeping applied voltages in the ±100 mV range using the PA before

the high-speed measurement (Figure 3.8). Linear current-voltage (*I-V*) characteristics obtained suggesting good contacts. Total resistance (including GST cell resistance, contact resistance, 1 kΩ of load resistance and metal extension resistance) is found using the slope of linear regression of the *I-V* characteristics.

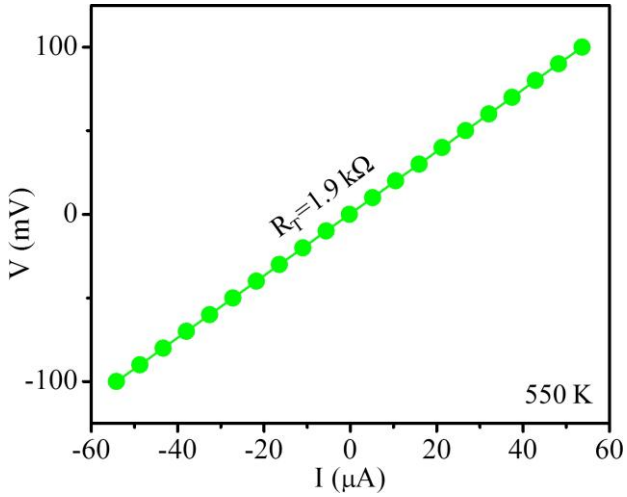


Figure 3.8. Example *I-V* characteristic based on the DC measurements using the PA to extract initial crystalline (hcp) GST line cell. The total resistance (R_T) includes load, contact, metal extension and GST line cell resistances.

Second, DAQ card is used to measure initial crystalline (hcp) cell resistances before the high-speed measurement using 50 mV DC baseline voltage applied by the FGU as seen in the first ~40 seconds in Figure 3.9.

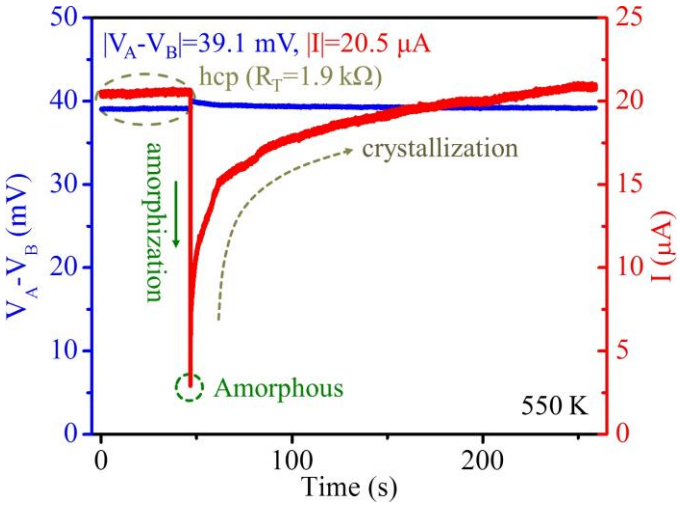


Figure 3.9. Example of voltage and current acquired by the DAQ card on a crystalline (hcp) GST line cell. The total resistance (R_T) includes load, contact, metal extension and GST line cell resistances.

Third, 1 MHz sinusoidal signal with amplitudes increasing from 50 mV to 100 mV in 3 steps applied by the FGU during the high-speed measurement. Each amplitude is applied for 26 µs (Figure 3.10).

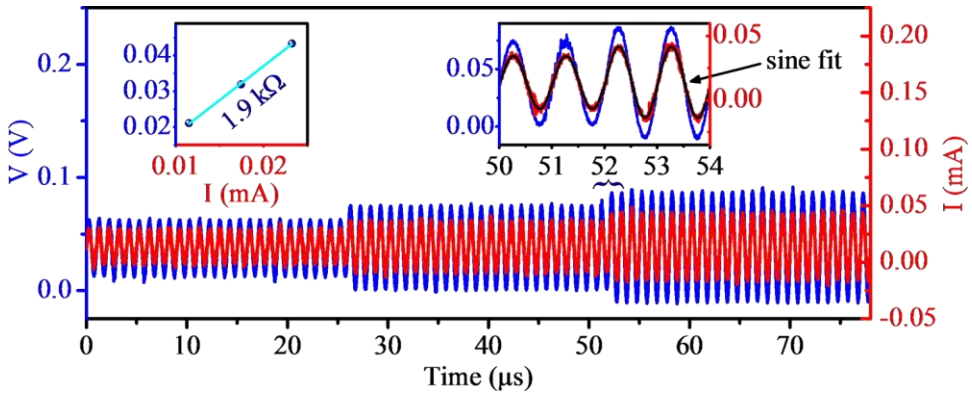


Figure 3.10. Example of applied and measured electrical signals for a high-speed measurement showing voltage and current on a crystalline (hcp) GST line cell before the melting pulse at 550 K. Insets show zoomed-in view of the signals and resistance calculation from the amplitudes of the sinusoidal fits.

The total resistances (R_T) in crystalline (hcp) phase are measured as ~1.5-2.5 kΩ, depending on the device size, which includes GST cell resistance (R_{GST}), contact resistance (R_X = ~100 Ω at 500K), 1 kΩ of load resistance and metal extension resistance (R_M = ~200 Ω at 300 K and ~230 Ω at 673 K). All three methods resulted in less than 5% variation in resistance for each device.

ii) Liquid cell resistances are measured during the 1 μs melting-pulse with stepwise increasing amplitudes in 8 steps applied by the FGU during the high-speed measurement. Applied pulse amplitudes are chosen for each device to be large enough to melt the device at first step and yet small enough to not to break the line cells, based on device dimensions (Figure 3.11). Melting pulse is followed by a 0 V bias for 1 μs to cool the cells down to chuck temperature and amorphize them.

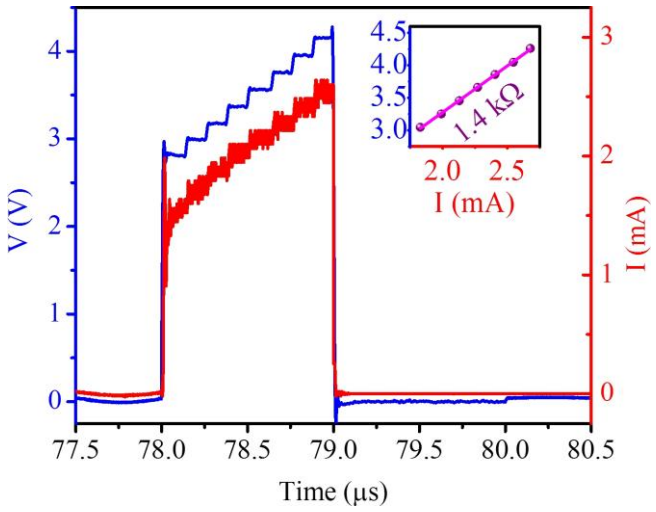


Figure 3.11. Example of applied and measured electrical signals showing voltage and current on a liquid GST line cell (during pulse) at 550 K. Inset shows the resistance calculation from the linear fits of the amplitudes.

Total device resistance in liquid phase is measured as ~1.4-2 kΩ, which includes GST cell resistance (R_{GST}), contact resistance (R_X = ~100 Ω at 500 K), 1 kΩ of load resistance and metal extension resistance (R_M = ~200 Ω at 300 K and ~230 Ω at 673 K).

iii) Amorphous cell resistances are measured using two methods:

1 MHz sinusoidal signals with first increasing amplitudes from 10 mV to a large value (0.1 to 2.2 V depending on the chuck temperature) in 20 steps and then decreasing amplitudes back to 10 mV in 20 steps applied by the FGU during the high-speed measurements for each temperature point. Each amplitude is applied for 48 µs (Figure 3.12).

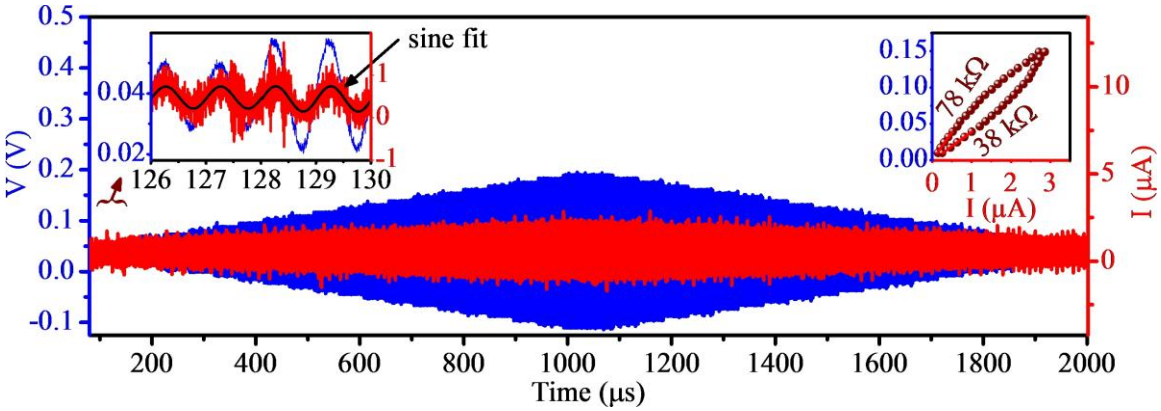


Figure 3.12. Example of applied and measured electrical signals showing voltage and current on an amorphized GST line cell (after pulse) at 550 K. Insets show zoomed-in view of the signals and resistance calculation from the amplitudes of the sinusoidal fits.

Amorphous cell resistances are also measured sweeping applied voltages in the ±100 mV range using PA, minutes after the high-speed measurement for low chuck temperatures ($T \leq 400$ K) (Figure 3.13). This method gives highly sensitive results however it is too slow and the material resistance drifts over time. Hence, resistivity is extracted by extrapolating the DC measurement results to 1 ms, to account for the

resistance drift in amorphous phase and to compare results from AC high-speed measurements.

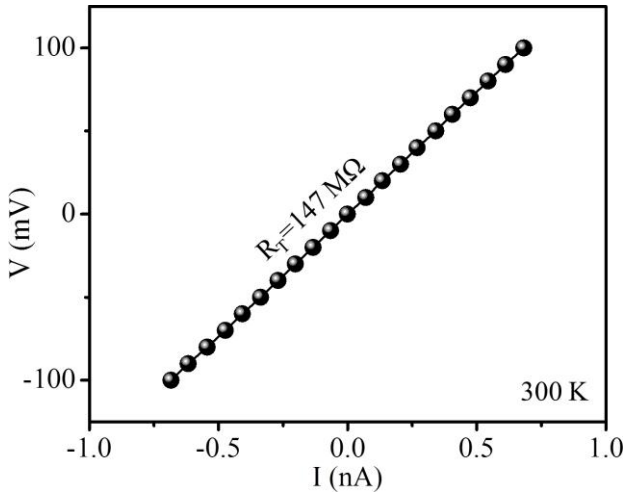


Figure 3.13. Example *I-V* characteristic based on the DC measurements using the PA to extract amorphous GST line cell resistance. The total resistance (R_T) includes load, contact, metal extension and GST line cell resistances. The *I-V* characteristics are observed to be very linear in this voltage range.

For higher chuck temperatures (T ~400-550 K), the amorphized cells transition to crystalline (fcc) over time (~hours). Some of these fcc cell resistances (at 425, 450 and 500 K) are measured sweeping the applied voltages in the ±100 mV range using the PA as they are slowly cooled down to 300 K (Figure 3.14).

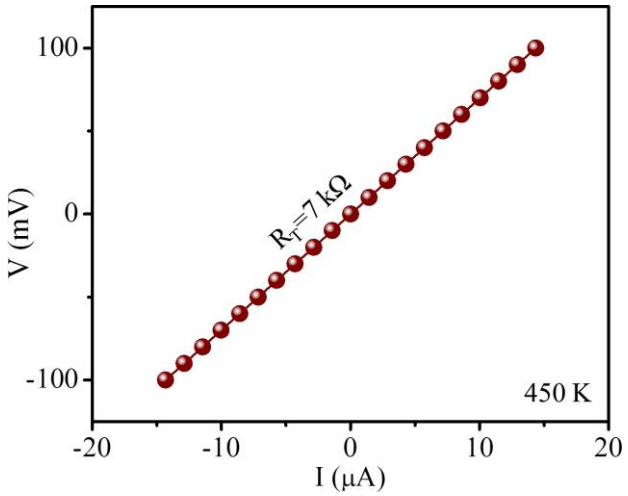


Figure 3.14. Example *I-V* characteristic based on the DC measurements using the PA to extract crystalline (fcc) GST line cell resistance. Sample was annealed at 450 K. The total resistance (R_T) includes load, contact, metal extension and GST line cell resistances. The *I-V* characteristics are observed to be very linear in this voltage range.

Typical slow *R-T* measurements on an as-fabricated (fcc) cell and two amorphized cells are also performed by continuously sweeping the applied voltages in the ±100 mV range while varying chuck temperature from 300 K to 675 K with 3.5 K/min heating rate and 125 K to 675 K with 1 K/min heating rate using the PA (Figure 3.15). Results from these slow *R-T* measurements are in good agreement with previous reports [2, 3, 6, 10, 14, 18, 39, 62, 63].

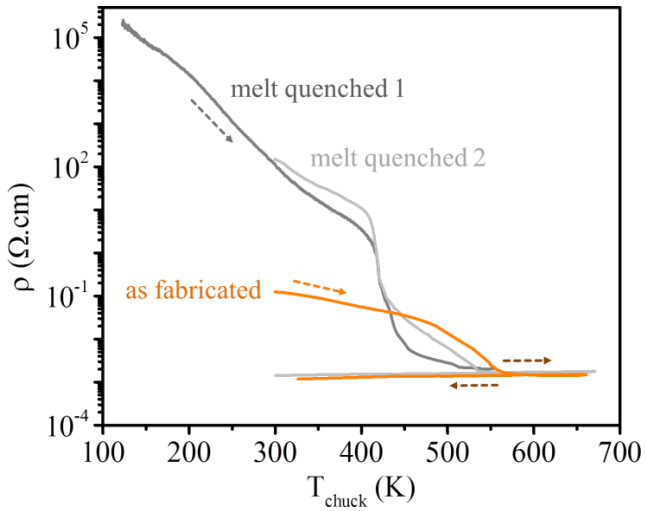


Figure 3.15. Measured GST resistivities as a function of temperature from slow *R-T* measurements (with 1-3.5 K/min heating rate) on three line cells.

Figure 3.16 summarizes the measurement procedure.

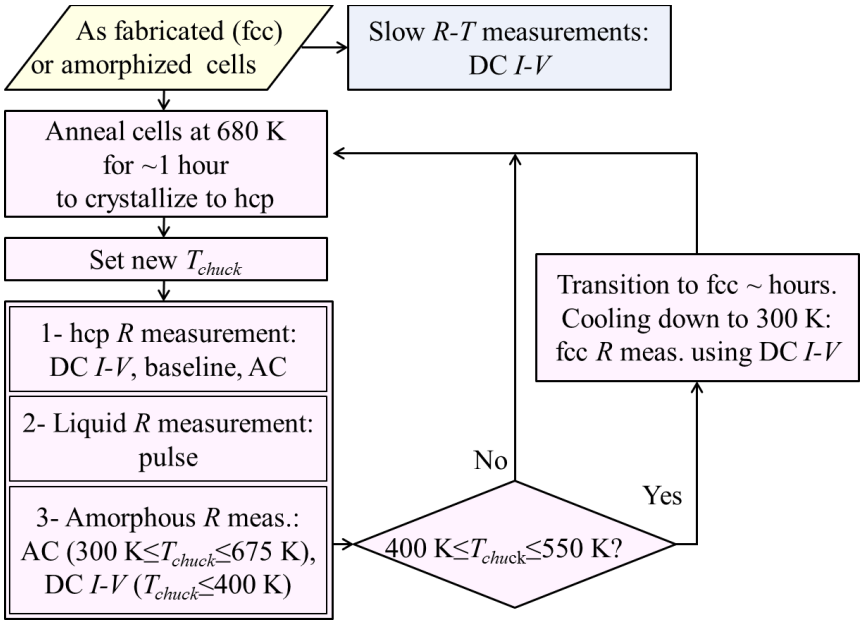


Figure 3.16. Flow chart depicting the measurement procedure.

3.4 Modeling of the measurement circuit

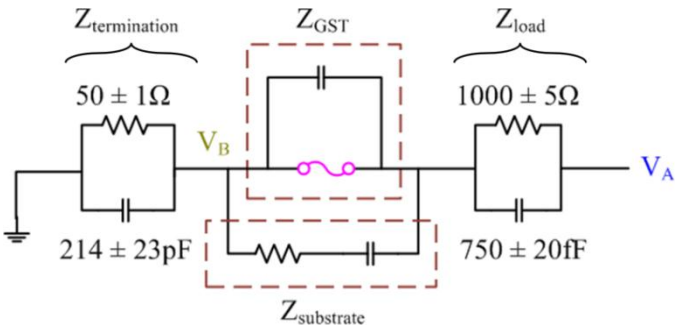


Figure 3.17. High-speed measurements circuit model used to calculate the resistance of GST line cells from the measured voltages V_A and V_B.

The resistance values of GST line cells are calculated using a circuit model of the experiments (Figure 3.17). The inductance of the circuit elements and coaxial cables used in the experiments is negligibly small. The total complex impedance of the circuit is calculated using the voltage drop across the whole circuit (V_A) and termination impedance (V_B). Measurement errors in V_A and V_B are calculated using sinusoidal fit errors which are typically very small. Noticeable fluctuations observed at low temperatures are possibly due to changes in conduction during nucleation of crystalline sites which serve as traps and once charged lead to coulomb blockade. Figure 3.18a,b shows measured V_B and V_A (with errors) on a GST line cell at 300 and 600 K. As an example, V_A and V_B values for the 10^{th} step (half maximum) are provided in Table 3.1, showing very small errors in these voltage readings.

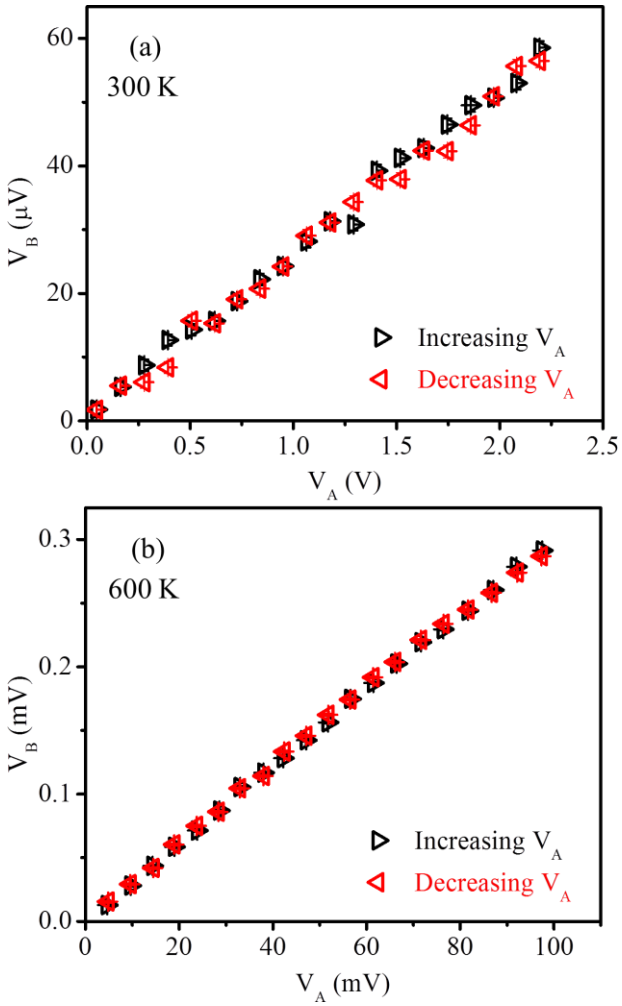


Figure 3.18. Example V_B versus V_A plots for a GST line cell during the 2 ms high-speed AC measurement (with increasing and decreasing sinusoidal signal amplitudes) following the melting pulse at 300 K (a) and 600 K (b).

Table 3.1. Samples of V_A and V_B values calculated using the sinusoid fits for the 10th step of the AC signals at 300 K and at 600 K.

	T = 300 K	**T = 600 K**
V_A	1.06 sin(ωt) (V)	(47.12±0.08) sin(ωt) (mV)
V_B	(28.14±0.94) sin(ω(t+190 ns)) (μV)	(142.22±0.73) sin(ω(t-2 ns)) (μV)

The phase difference between V_A and V_B readings is large (2π x 190 ns/1 μs) for low temperatures at which the substrate impedance, almost purely capacitive, dominates the current path. This large phase difference gives rise to a larger capacitive (imaginary) current than the resistive (real) current:

$$I\angle\phi_I - \phi_A = \frac{V_B\angle\phi_B - \phi_A}{Z_{termination}} \tag{3.3}$$

Figure 3.19 shows corresponding imaginary and real current plots for 300 and 600 K. The imaginary current is much larger than the real current at 300 K owing to the large GST line cell resistance, hence the large phase difference between V_B and V_A. The real component of current overwhelms the imaginary component at high temperatures. The total conductance of the circuit is found using slope of linear regression for current (I) versus V_A characteristics. Errors in the current, coming from the V_B readings, and uncertainties in the termination impedance are used as weighting factors for the linear regressions. However, inclusion of these errors does not change the obtained conductance values, as these errors are very small (< 1%).

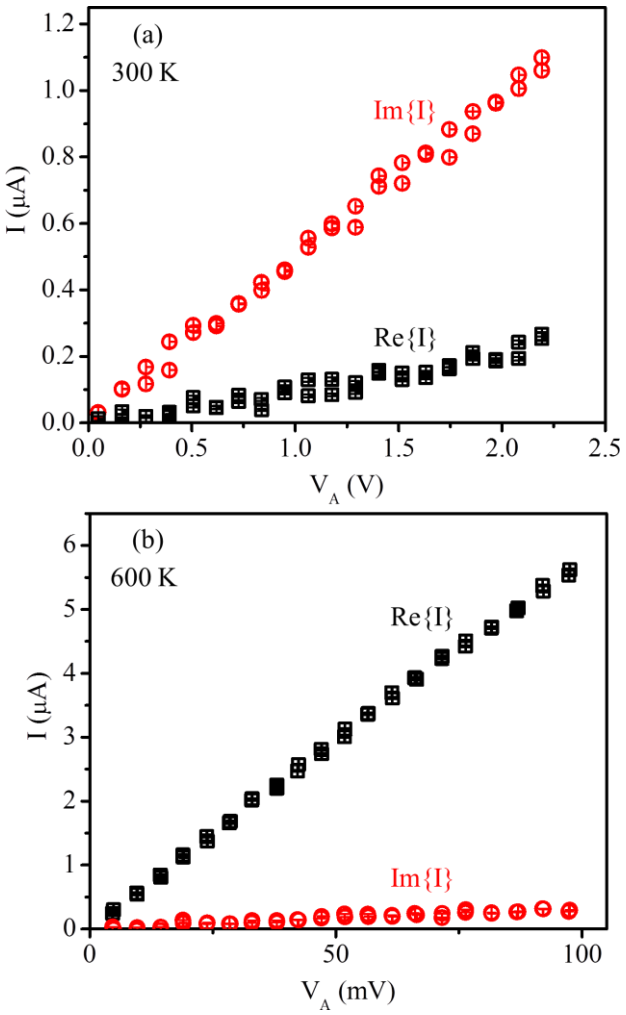


Figure 3.19. Real and imaginary components of current as functions of applied voltage (V_A) at 300 K (a) and 600 K (b) for the same examples in Figure 3.18.

The total impedance of the circuit is calculated using the imaginary and real components of the conductance values (Equation 3.4). Errors in the conductance values, coming from the linear regression process, are propagated to calculate the errors in the total impedance:

$$Z_{total} = \frac{1}{Re\{Conductance\} + j\ Im\{Conductance\}} \qquad (3.4)$$

Table 3.2. Real and imaginary components of the total impedances at 300 K and 600 K for the same examples in Figure 3.18.

	***T* = 300 K**	***T* = 600 K**
$Z_{total\text{-}Real}$	0.43±0.01 MΩ	17.27±0.03 kΩ
$Z_{total\text{-}Imaginary}$	-1.97±0.02 MΩ	-1.06±0.00 kΩ

Table 3.2 shows calculated Z_{total} for the same example GST line cell. Once Z_{total} is found, the GST line cell impedance is calculated using known load, termination and substrate impedances:

$$Z_{GST} \,//\, Z_{substrate} = Z_{total} - Z_{load} - Z_{termination} \tag{3.5}$$

The substrate impedance ($Z_{substrate}$) and errors associated with it are measured on large number of broken line cells using the same model at all chuck temperatures. An average value of (-370±50) kΩ + j (-4.8±0.1) MΩ is used for the calculations (Figure 3.20, Table 3.3). Although the real part of $Z_{substrate}$ is negative, results from the AC measurements using this model are close to the more reliable DC measurement results. The errors/uncertainties in these impedances are propagated to calculate the errors in GST cell impedance. A capacitor in parallel with the GST line cell is introduced in the model to account for any remaining complex component in the GST line cell impedance which is calculated to be typically small (< 1 pF). The errors in GST line cell impedance are dominated by the uncertainties in $Z_{substrate}$ as the errors/uncertainties associated with the other circuit elements and measurements are very small. Table 3.4 shows the calculated resistance and capacitance for the same example GST line cell.

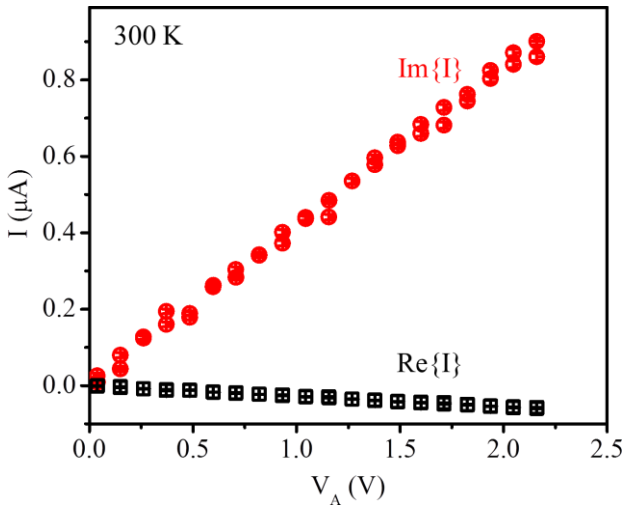


Figure 3.20. Real and imaginary components of current as functions of applied voltage (V_A) on a broken wire at 300 K.

Table 3.3. Real and imaginary components of the substrate impedance at 300 K for the same example in Figure 3.20.

	***T* = 300 K**
$Z_{substrate\text{-}Real}$	-0.37±0.05 MΩ
$Z_{substrate\text{-}Imaginary}$	-4.8±0.1 MΩ

The extracted total resistance (R_T) includes the GST line cell resistance (R_{GST}), contact resistance (R_X) (~100 Ω at 500K), and metal extension resistance (R_M) (~200 Ω at 300 K and ~230 Ω at 675 K) (Equation 3.6). Resistivity of GST line cells are calculated using the actual device dimensions length (*L),* width *(W),* and thickness *(t)* (as measured using SEM) (Equation 3.7).

$$R_T = R_{GST} + R_X + R_M \tag{3.6}$$

$$R_{GST} = \rho \frac{L}{Wt} \tag{3.7}$$

The Matlab codes used to model the circuit are given in Appendix 5.5.

Table 3.4. Calculated resistances and capacitances at 300 K and 600 K for the same examples in Figure 3.18.

	***T* = 300 K**	***T* = 600 K**
R	7.7±1.0 MΩ	16.3±0.7 kΩ
C	16±4 fF	570±170 fF

We confirmed the accuracy of the AC high-speed measurement results by comparing them to highly sensitive DC *I-V* measurement results. The results from the AC high-speed and DC *I-V* measurements are in good agreement for GST line cell resistances up to ~100 MΩ using this model (Figure 3.21). Resistance of typical GST line cells used in AC high-speed measurements are in the order of 40 MΩ in the amorphous phase at room temperature. Very high resistance values (~100-400 MΩ) shown in Figure 3.21 are from the drifted GST line cells.

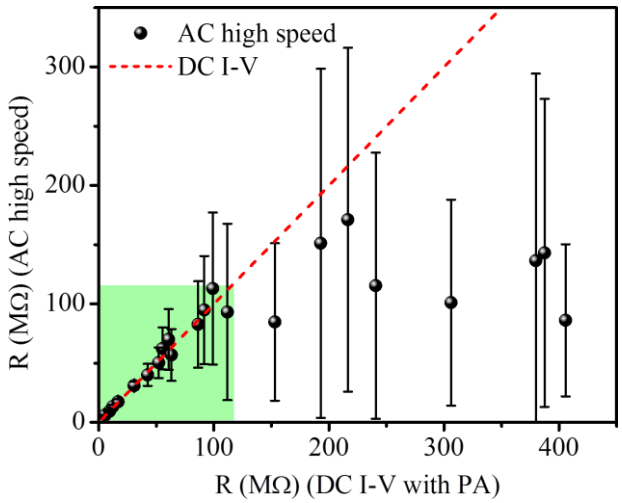


Figure 3.21. Comparison between AC high-speed measurement and DC *I-V* measurement results shows good agreement up ~100 MΩ GST line cell resistances.

3.5 Crystallization of GST phase change memory devices

The data captured by the oscilloscope (the first 2 ms) and the DAQ card (starting at ~10 ms) are aligned (time-shifted) using the melting pulse as the reference, which corresponds to the sudden increase in resistance (Figure 3.22a).

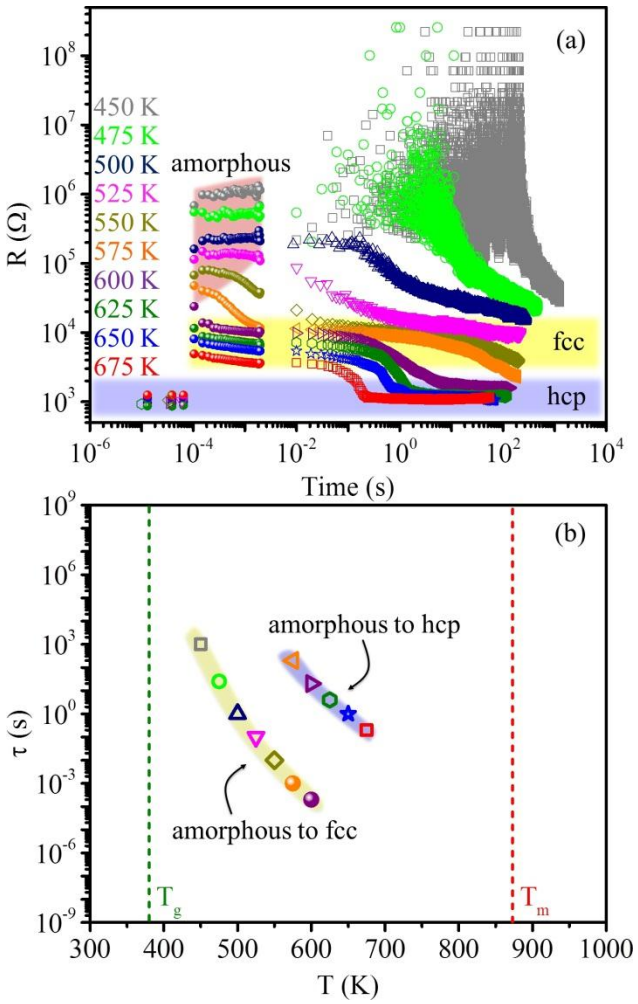


Figure 3.22. Resistances calculated from the AC high-speed measurements (solid symbols) and long duration DC baseline measurements (open symbols) for a single device. Amorphization pulse starts at 78 μs, followed by 1 μs 0V cool-down period and AC signal starts at 80 μs (a). Approximate crystallization times from amorphous to fcc in 450-600 K and from amorphous to hcp in 600-675 K temperature ranges with corresponding colors and symbols (b).

The amorphous-fcc-hcp phase transitions are fully captured in the T_{chuck} = 550-600 K range. The amorphous-fcc transition is significantly faster at elevated temperatures, $\tau_{a\text{-}fcc}$ < 20 µs for T_{chuck} > 600 K. However, resistivity is also lower (better signal to noise ratio), making it possible to capture this transition at elevated temperatures using shorter sinusoid segments.

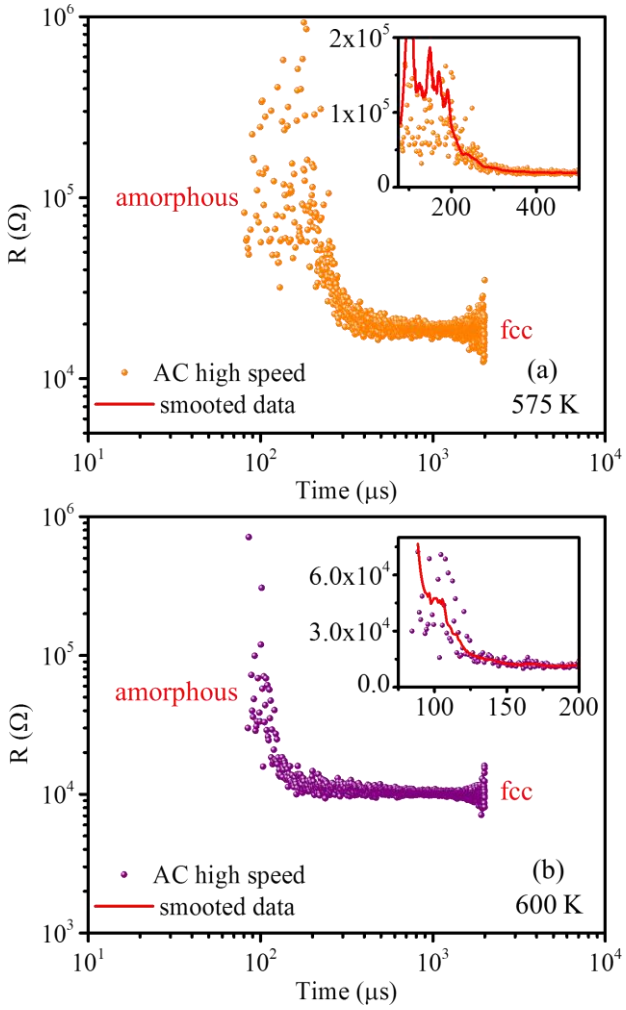


Figure 3.23. 4 MHz AC high-speed measurements performed at 575 K (a) and 600 K (b). Insets are the zoomed-in views of resistance change during amorphous to fcc transition (in the order of 100 µs). Amorphization pulse starts at 78 µs, followed by 1 µs 0V cool-down period and AC signal starts at 80 µs.

Since the crystallization times are fast (in the order of 100 μs) between 550 K and 600 K, higher frequency sinusoidal signals (4 MHz instead of 1 MHz) are used on another set of GST line cells to construct sufficient *I-V* curves using amplitudes of sinusoidal fits in this short duration. Beyond 600 K the material crystallizes in the order of a μs (Figure 3.23), hence a faster characterization technique is required.

The fcc-hcp phase transitions are observed to be slow ($\tau_{fcc\text{-}hcp}$ ~200 s to 0.2 s) for 575-675 K range and can be fully captured in long duration measurements using the DAQ card (Figure 3.22). Since the PCM devices are not expected to experience the hcp phase during normal (high-speed) operation and the ambient temperature is below the fcc-hcp transition, this transition is not of significant interest for most cases.

3.6 Resistance drift in amorphous GST phase change memory devices

It has been reported that the amorphous GST resistance increases over time - resistance drift- in time due to change in band gap or decrease in defects states caused by structural relaxation, or changes in the activation energies caused by crystallization [2, 3, 5, 6, 26-30]. The long-term stability of amorphous phase and amorphous-fcc transition is critically important as the resistance drift over time hinders the possibility of multi-bit/cell storage and increases variability. We have used a quasi-static approach and a parameter analyzer to characterize very long-term resistance drift for $T < 500$ K, up to 13 months (~$3\text{x}10^7$ s) at 300 K. The resistance is observed to follow a power law, $\rho_{a\text{-}GST} \sim t^n$ (Figure 3.24a), n decreasing with T (from 0.1 at 300 K to 0.04 at 450 K) (Figure 3.24b) and $\rho_{a\text{-}GST}$ shows a clear maximum and turn around for $T_{chuck} > 350$ K as seen in Figure

3.24a and for room temperature as seen in Figure 3.25. The power-law behavior is attributed to contributions from a number of different mechanisms with various activation energies. Large numbers of line cells were measured for each temperature (300-450 K) to determine resistance drift behavior.

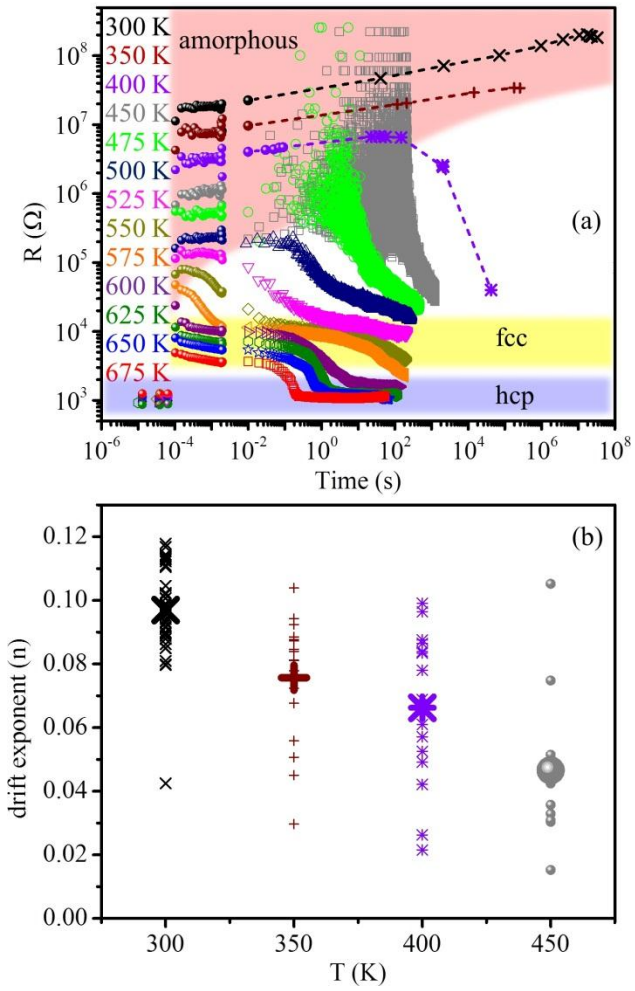


Figure 3.24. Resistances calculated from the high-speed measurements (solid symbols) and long duration DC baseline measurements (open symbols) for a single device. Dashed lines indicate resistance change in amorphous phase and crystallization process for low temperatures (300-400 K). Amorphization pulse starts at 78 μs, followed by 1 μs 0V cool-down period and AC signal starts at 80 μs (a). Drift exponent (*n*) as a function of temperature (b).

The 26 devices measured for very long duration (~13 months) show a consistent trend in resistance drift at room temperature (~300 K) (Figure 3.25a,b). Their resistances have reached to maximum and turned around at ~4 months after the amorphization. The decrease in resistance after reaching the maximum is slower on wider structures (Figure 3.25c).

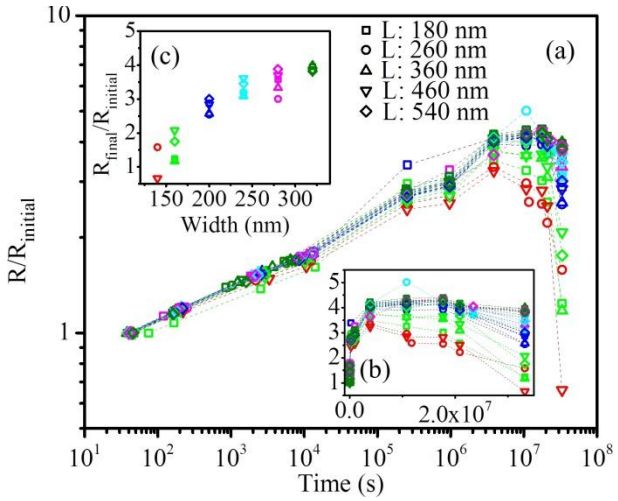


Figure 3.25. Normalized resistance as a function of time at 300 K in log (a) and linear (b) scales. $R_{final}/R_{initial}$ values as a function of device width for various lengths (c).

The resistance drift is observed in a shorter time period at higher temperatures and material is observed to be crystallized in a few seconds at ~450 K. Higher frequency sinusoidal segments (4 MHz instead of 1 MHz) are used on another group of GST line cells to capture resistance drift in short duration at 450 K (Figure 3.26).

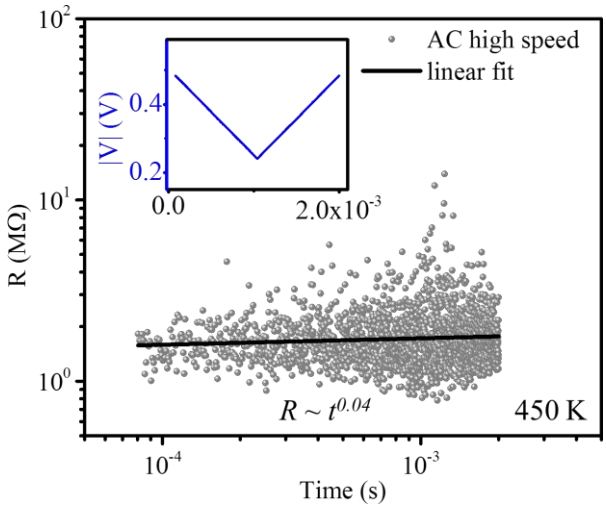


Figure 3.26. Resistance drift at 450 K using 4MHz AC high-speed measurements. Amorphization pulse starts at 78 μs, followed by 1 μs 0V cool-down period and AC signal starts at 80 μs. Inset is the amplitudes of the sinusoidal segments used after the pulse.

Experimental results suggest that the material starts nucleating soon after amorphization as it relaxes, even at room temperature, in-line with earlier observations of nano-crystals in melt-quenched GST [18, 94, 95]. The mechanical strain induced by the crystalline nuclei is expected to promote defect formation and increase in the band-gap of amorphous GST. These defects and the surface states at the crystalline-amorphous interfaces contribute to temporary trapping of charges [96]. As the crystalline grains grow larger (~5 nm) [5], the crystalline islands tend to behave more like bulk fcc (degenerate narrow-band-gap semiconductor) and form potential wells that can capture free carriers. Both the traps and the nuclei are expected to decrease the free carrier lifetimes and charging of these sites by the captured carriers distort the potential profile giving rise to Coulomb blockade [97, 98]. Since the cells are small and highly resistive, the blockade caused by a single trapped charge can be very significant (Figure 3.28c). Estimation of

the local potential changes caused by these charged nuclei is performed with 2D simulation using Synopsys TCAD (Figure 3.27).

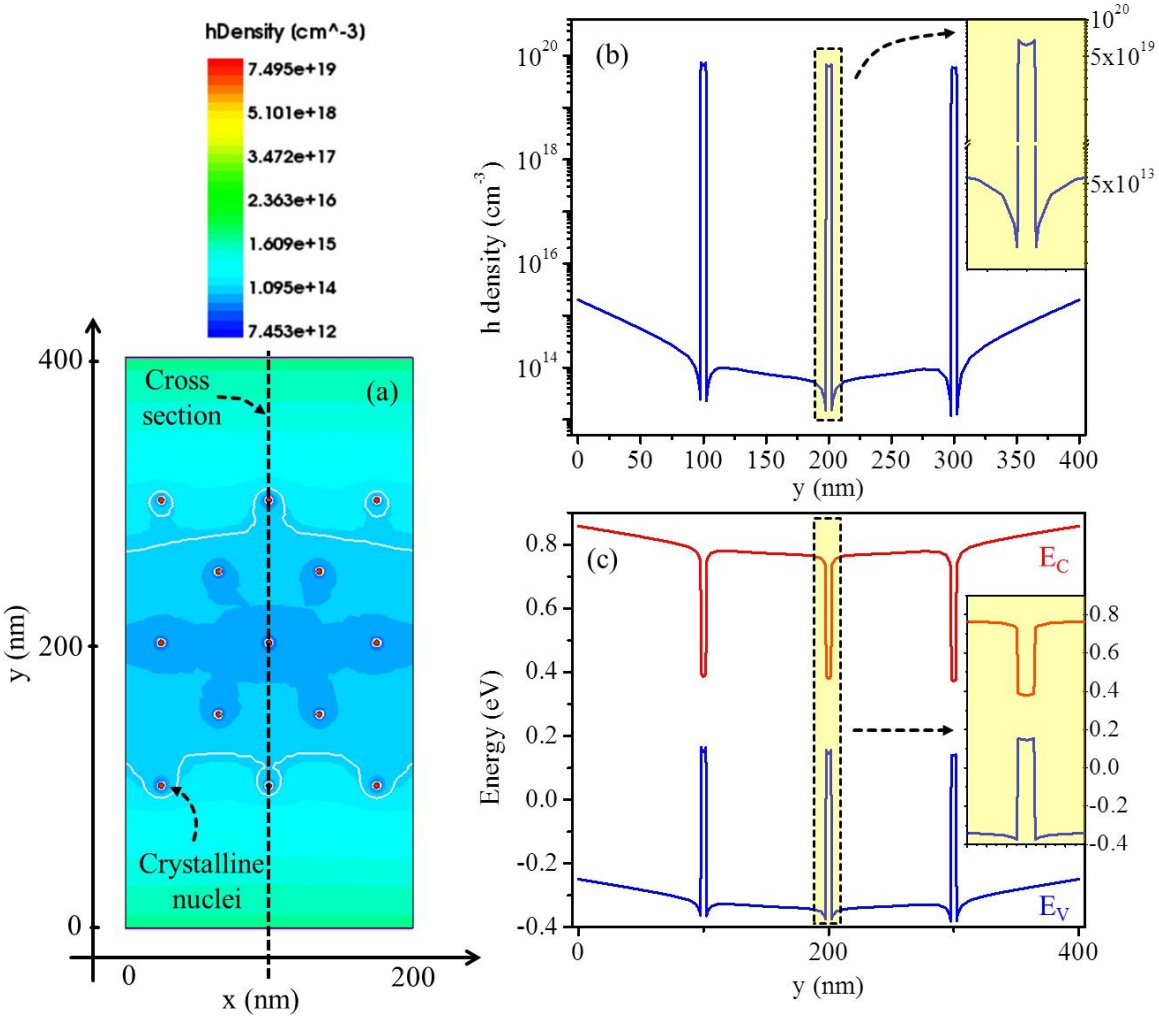


Figure 3.27. 2D simulations of 13 circular (5 nm diameter) crystalline nuclei inserted into a 200x400 nm amorphous block using Synopsys TCAD tool. Each nucleus is modeled as a bulk fcc GST layer with a charge density of $5x10^{19}$. A band bending of ~0.1 eV is observed. Capacitive coupling between the nuclei and the surrounding device contacts determine the overall capacitance and hence the potential perturbation ($Q_{trapped} = C_{nuclei} V_{perturbation}$). Hole density profile (a). Hole density along the cross section (b). Band diagram along the cross section (c). Insets are the zoomed-in view around center nuclei (Simulations are performed by Nicholas Williams).

These processes associated with initial stages of crystallization can be the dominant factors giving rise to resistance drift (increase) and fluctuations over time. With the increasing number and size of the nuclei, conduction through the crystalline islands starts playing a more significant role. As the current percolation through the nanocrystals is initiated at ~30% crystalline ratio, a significant reduction in electrical resistivity is observed when this threshold is reached during the crystallization process (Figure 3.28d-f) [18, 23, 94, 95, 97-100].

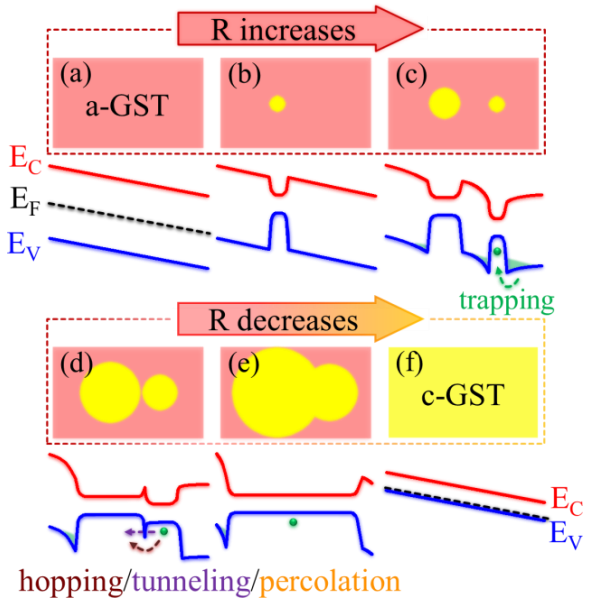


Figure 3.28. Schematic illustration of resistance drift due to nucleation (a, b), capture of free holes and distortion of the potential profile (c), growth of the crystalline nuclei leading to initiation of percolation transport (d, e) and complete crystallization resulting in decrease in resistance (f). Grain boundaries are not shown.

3.7 Electrical resistivities of metastable amorphous and crystalline (fcc) GST

Large number of devices were measured for each temperature point to determine the resistivity characteristics in liquid, crystalline (hcp and fcc), and amorphous phases of GST using this high-speed technique (Figure 3.29). The metastable $\rho_{a\text{-}GST}$ is found to be 50 to 400 times larger than the slow *R-T* measurement results in 425-600 K temperature range and the metastable $\rho_{fcc\text{-}GST}$ is found to be 15 to 20 times larger than the slow *R-T* measurement results in the measured temperature range of 550-675 K.

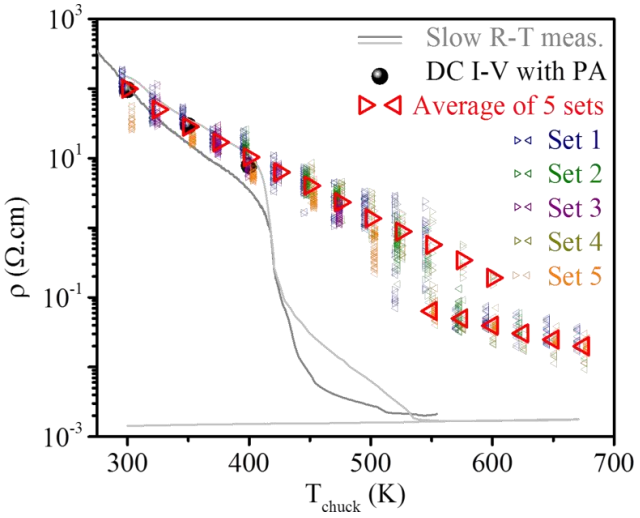


Figure 3.29. Distribution of measured amorphous and fcc GST resistivities as a function of temperature. Solid lines show slow *R-T* measurements (with 1-3.5 K/min heating rate) on two line cells. Symbols show AC high-speed measurement results at a constant chuck temperature corresponding to the metastable amorphous and fcc phases resistivities. Each data points (large red symbols) are from average of data collected from large number of line cells from 5 set of samples. Small symbols represent to individual measurements corresponding to total of ~1700 measurements.

Carrier activation energies (E_a) calculated using the high-speed and slow *R-T* measurement results are ~0.2-0.3 eV in 250-450 K range, possibly due to activation of

traps (Figure 3.30) [2, 27, 29, 97]. At least three distinct E_a, suggesting different dominant processes at various temperature ranges, are observed at higher temperatures. At higher temperatures, the material is likely to have nucleated while the measurements are being performed. Hence, the higher activation energy processes observed here may be due to detrapping of holes from the nuclei which eliminates the blockade region surrounding those nuclei. The distinct increase in E_a around 550 K to 0.6 eV may be due to increase in average nuclei size: Nuclei behaving more like bulk fcc GST wells with a valence band offset of 0.6 eV in reference to surrounding amorphous GST, rather than behaving like smaller quantum dots with available energy levels closer to the valence band edge of a-GST [26, 97, 101]. While it takes time for the nuclei to form and grow to several nanometers, and carrier activation associated with the nuclei would not be relevant for growth-driven set operations, it is possible to have a pre-nucleated amorphous GST in the reset state for rapid crystallization. This can be achieved by adjusting the tail of the reset pulse to promote nuclei formation immediately after amorphization. This increases the time and energy associated with reset operation but significantly reduces the time needed for set. Hence, the time and the energy associated with reset and set operations can be balanced out by pre-nucleation.

Metastable fcc phase is expected to be polycrystalline with small grains and the activation energy calculated for the metastable fcc phase, ranging from 0.25 eV at 550 K to 0.35 eV at 650 K, is expected to correspond to carrier injection through the potential barriers at the grain-boundaries [27, 29]. Increased thermal energy enables contribution of grains that are isolated with higher or wider potential barriers, broadening the percolation paths.

All resistivity values (liquid, crystalline (hcp and fcc), and amorphus) obtained from this work are listed in Appendix 5.6.

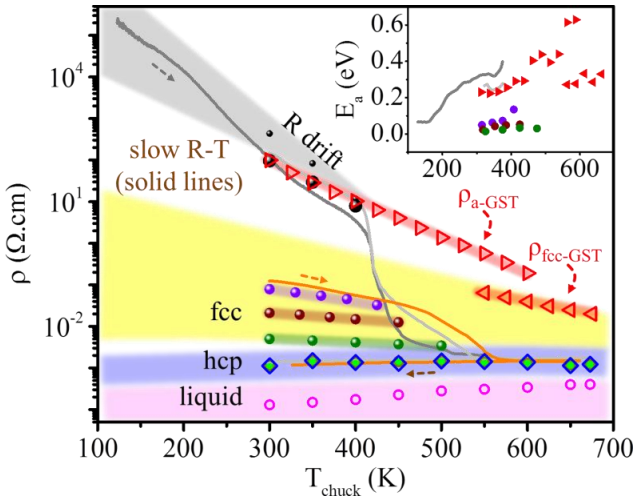


Figure 3.30. Temperature dependent electrical resistivity and activation energy of GST. Solid lines show slow *R-T* measurements (with 1-3.5 K/min heating rate) on three line cells. Symbols show measurement results at a constant chuck temperature (solid symbols are from DC measurements, open symbols are from high-speed measurements). Each data point is an average of data collected from large number of line cells (total of ~1700 measurements). Inset shows calculated activation energies associated with carriers, with the corresponding colors and shapes. The direction of the triangles indicate the voltage stepping up (▷) and down (◁).

3.8 Quasi-static approach (DC high-speed measurements)

We have performed quasi-static measurements using a similar experimental setup (Figure 3.31). At lower temperatures (T < 500), device resistance in the amorphous state is very high, hence we have used a large termination resistance (1 MΩ) to obtain readable current levels. Due to the longer *RC* time constant (~150 μs) induced by the large termination resistance, quasi-static measurements require a longer measurement duration (20 ms) instead of 2 ms used for AC high-speed measurements (Figure 3.32a). At higher

temperatures ($T > 500$), device resistance is lower, thus a 50 Ω termination resistance is used. The reduced *RC* time constant (~7.5 ns) enables quasi-static measurements in 2 ms time scale (Figure 3.32b).

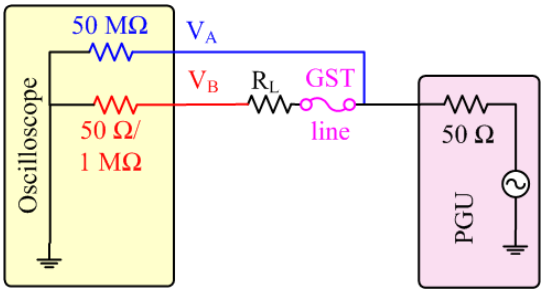


Figure 3.31. Schematic of the experimental setup for quasi-static measurements.

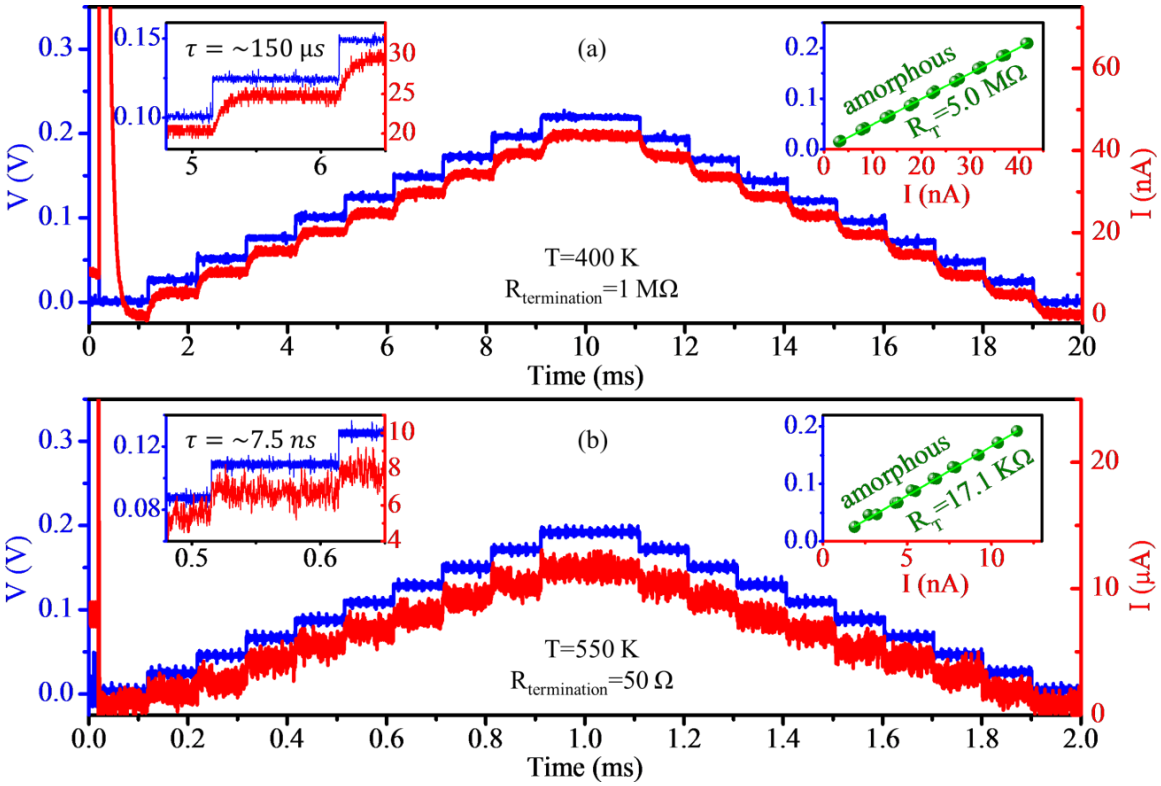


Figure 3.32. Samples of applied and measured signals showing voltage and current on GST line cells for the quasi-static measurements at T = 400 K using 1 MΩ termination (a) and at T = 550 K using 50 Ω termination (b). Insets show the zoomed-in view of the signals in amorphous (after pulse) phase and *I-V* characteristics obtained from DC signal steps.

Quasi-static measurement results are in good agreement with those of DC *I-V* measurements at low temperatures and AC high-speed measurements at elevated temperatures (Figure 3.33).

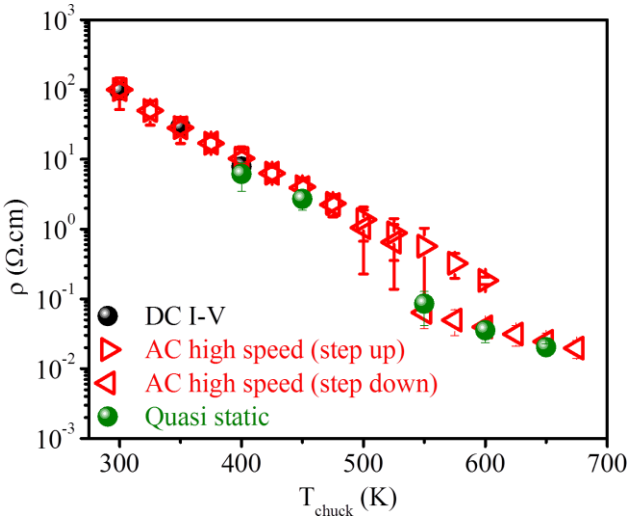


Figure 3.33. Comparison of the average metastable amorphous and fcc GST resistivities measured using DC *I-V*, quasi-static (DC high-speed)(solid green symbols), and AC high-speed measurement (open symbols) techniques.

3.9 Cycling of GST phase change memory devices

We have performed cycling measurements using another set of GST line cells. An Agilent 8114A pulse generator is used to apply pulses -reset pulse (6-9 V, 10-100 ns), set pulse (~4-5 V, 500 ns-1 μs) and read pulse (1 V, 1 ms)- and a Tektronix TDS724D oscilloscope is used to measure the applied voltage (V_A) and current (by measuring voltage across the 50 Ω (for reset and set) or 1 MΩ (for read) termination resistor) (Table 3.5). We have used the measurement setup shown in Figure 3.34a,b. A 5.1 kΩ load resistor is attached to the W probe tip to limit the current (Figure 3.34c). Sequence of electrical signals (reset, read, set, read) are continuously applied until the GST line cell breaks (Figure 3.34d).

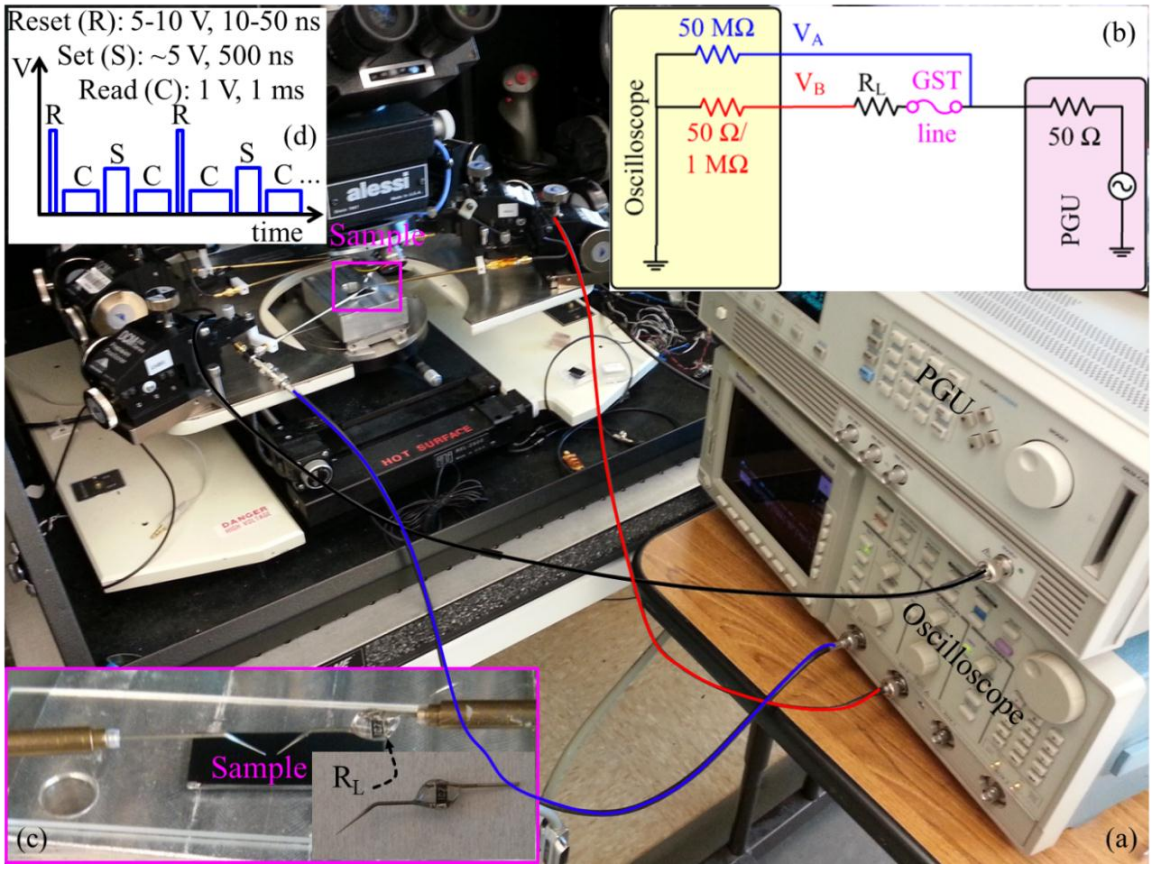


Figure 3.34. View of the experimental setup for cycling measurements (a). Schematic of the experimental setup (b). Surface mount load resistor attached to the probe tip to limit the current to avoid breakage(c). Schematic illustration of the applied signals (d).

Table 3.5. Example applied pulse (V_A) amplitudes and durations to cycle devices of different dimensions at 300 K.

Devices	Reset	Set
L200W70	9 V-100 ns	5 V-1 µs
L200W62	6 V-100 ns	4 V-1 µs
L190W108	9 V-10 ns	5 V-500 ns
L180W86	8 V-30 ns	4 V-1 µs

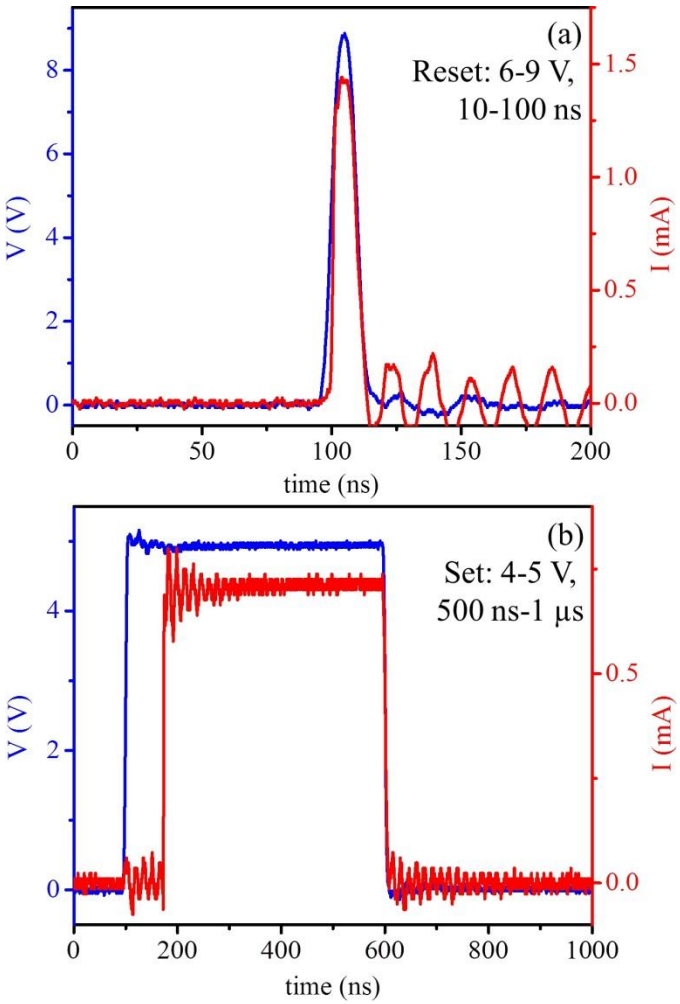


Figure 3.35. Example of measured voltage (V_A) and current (V_B/50 Ω) as a function of time for reset (a) and set (b) operations.

During these experiments, ~2-3 orders of magnitude resistance contrast is observed between amorphous and fcc phases when devices are cycled ~31-178 times (Reset: ~400 kΩ-40 MΩ and Set: ~4 kΩ-70 kΩ) (Figure 3.36).

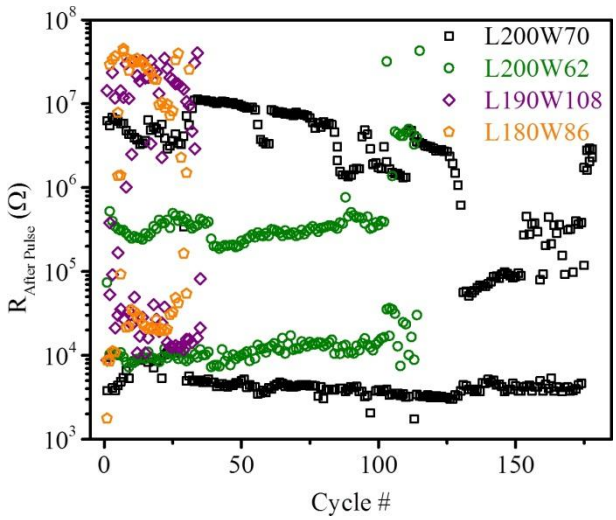


Figure 3.36. Reset and Set resistance values of devices with various dimensions cycled 31 to 178 times during the experiments. Some cycling attempts were failed and those data points are removed. *L:* 200 nm, *W*: 62 nm device is experienced lower pulse conditions, hence the resistance contrast is lower compared to others devices (Table 3.5).

3.10 Breakdown field of amorphous GST

We have crystallized amorphized GST line cells using a triangular set signal which is inserted in the last segment of the regular AC high-speed measurement. The triangular set signal is used to determine the breakdown field which corresponds to a sudden jump in current (Figure 3.37).

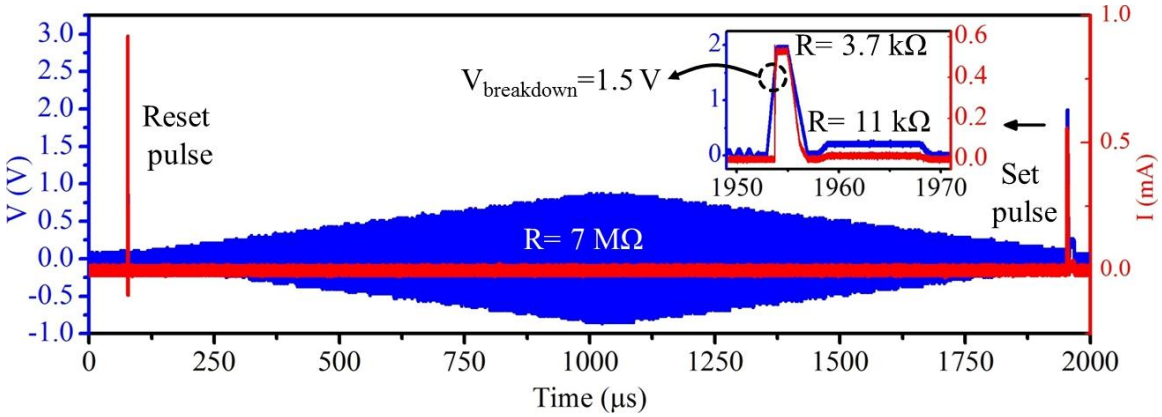


Figure 3.37. Example of applied and measured signals for breakdown field measurements. Inset is the zoomed-in view of the triangular set signal followed by a read signal showing voltage and current. Breakdown occurred at 1.5 V applied voltage and device is crystallized with final resistance value of 11 kΩ (T_{chuck} = 300 K).

Resistance values after amorphization pulse are measured using high-speed AC measurement technique. The length of the amorphized region is calculated using known electrical resistivity of metastable amorphous GST, defined device width and thickness (Equation 3.8). Calculated amorphized region length is used to calculate the electrical breakdown filed for amorphous GST (Equation 3.9). The breakdown field of amorphous GST measured from a large number of line cells (~100 devices) is ~52±21 V/μm at 300 K, in line with previously reported values (10-100 V/μm) (Figure 3.38) [3, 29, 102-105]. The final crystalline GST line cell resistance is measured using a small amplitude read signal following the set signal (Figure 3.37).

$$L_{Amorphized} = \frac{R_{GST} W t}{\rho} \tag{3.8}$$

$$E_{Breakdown} = \frac{V_{Breakdown}}{L_{Amorphized}} \tag{3.9}$$

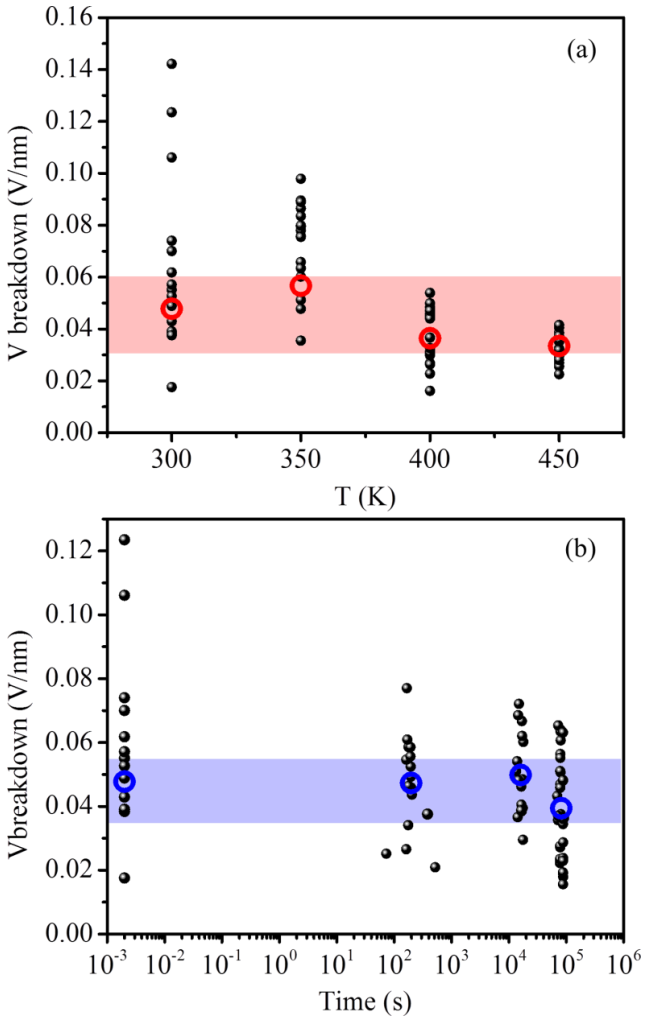


Figure 3.38. Breakdown field of amorphous GST as a function of temperature (a) measured on devices with various dimensions (*L*: 200-500 nm, *W*: 100-260 nm, *t*: 50 nm) and time (b) Large number of GST line cell (~100 devices) are used to determine breakdown field of GST (T_{chuck} = 300 K).

3.11 TEM analysis of measured GST phase change memory devices

Two of measured devices are picked up from the die using a FEI Strata dual-beam FIB (focus ion beam) system. TEM (transmission electron microscopy) analysis is performed using a JEOL JEM-2010 FasTEM system one day after amorphization. Both devices are amorphized using 300 ns long pulse where the amplitude is stepped from 3.5

to 4 V at 300 K using the high speed measurement technique (Figure 3.39a and Figure 3.41a). The first device is kept in amorphous phase for ~1 day (resistance of the device is drifted ~1 day).

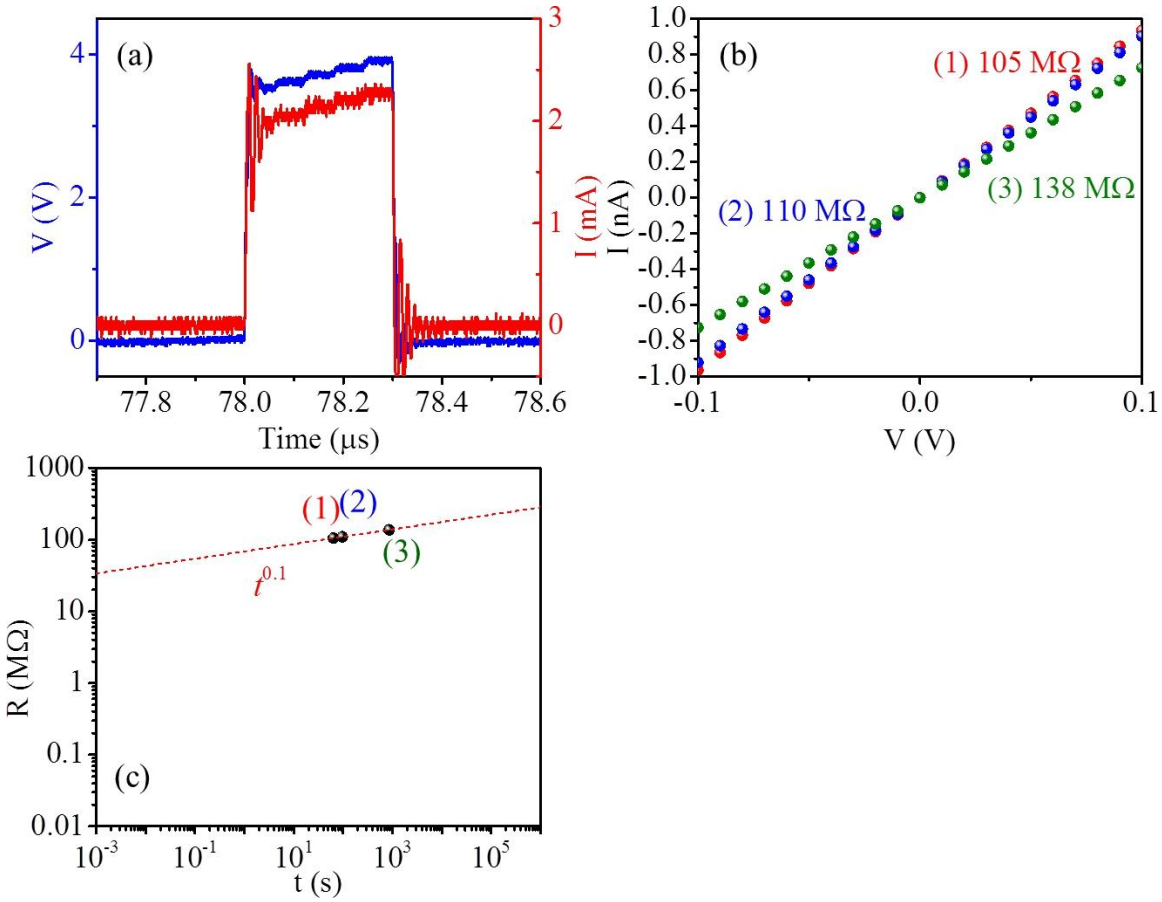


Figure 3.39. Applied and measured electrical signals showing voltage and current on a GST line cell (during pulse) at 300 K (a), *I-V* characteristics using PA at 300 K after amorphization at 64, 97 and 865 seconds (b), and resistance change as a function of time (c). The device is kept as is for TEM analysis.

Parameter analyzer is used to characterize the resistance drift (~40 min.). Electrical characteristics show linear *I-V* characteristics and a high resistance state (amorphous) is achieved (with ~150 MΩ final resistance) (Figure 3.39b,c). The non-

linearity observed in first *I-V* characteristics (at 64 seconds) (red symbols in Figure 3.39b) is due to the resistance drift during the voltage sweep (~10 s) and it is negligible.

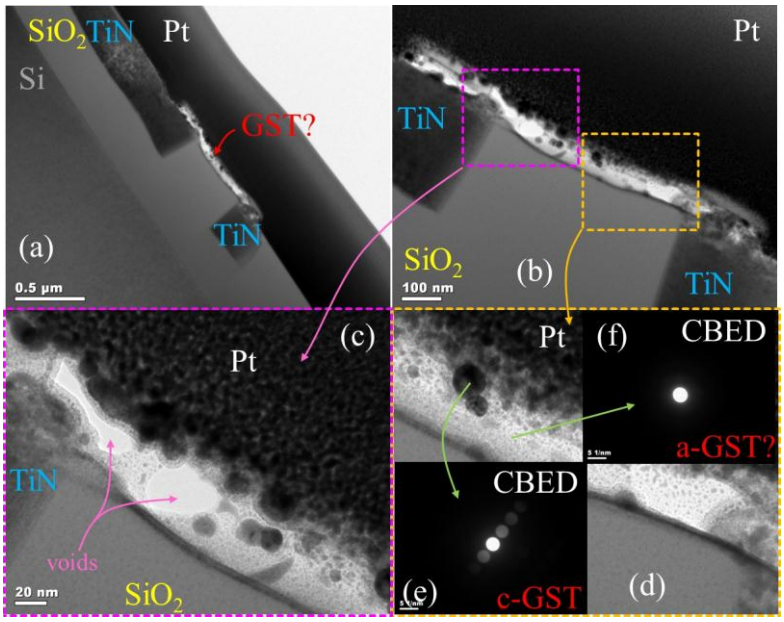


Figure 3.40. TEM images of an amorphized and drifted (~1 day) device (line section dimensions: *L*: ~320 nm, *W*: ~100 nm, *t*: ~50nm) (a-d), Converged beam electron diffraction patterns from the pointed areas (e,f). (TEM and CBED images are taken by Roger Ristau in IMS at UConn).

TEM images show non-uniform device structure, possible damaged during FIB milling and thinning process. However some crystalline grains with varying sizes are observed and amorphous and crystalline diffraction patterns are detected from pointed areas. Also, some voids are observed (Figure 3.40).

The second sample was crystallized to fcc phase by ramping up (~2.5 K/min) the hot-chuck to 470 K and annealing the device for 15 minutes at 470 K (Figure 3.41c,d).

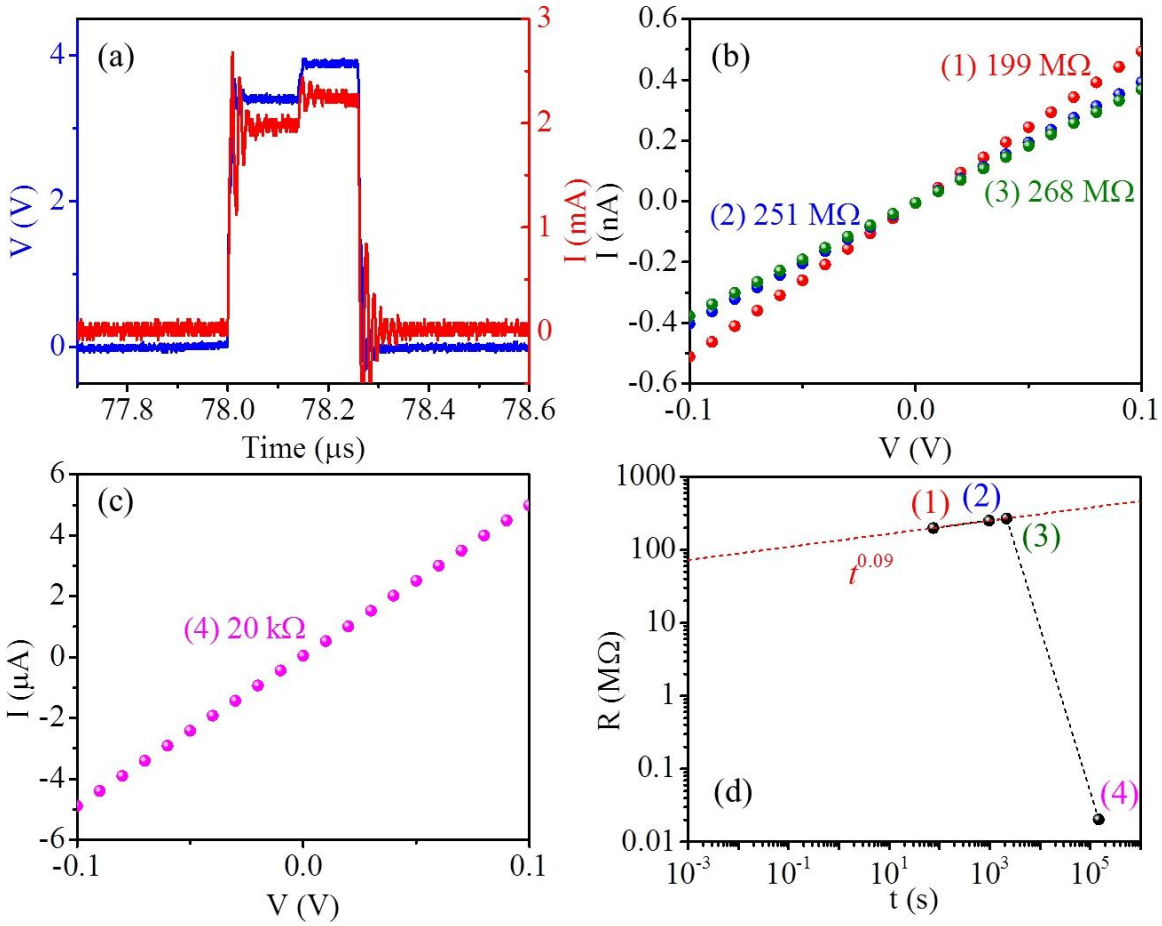


Figure 3.41. Applied and measured electrical signals showing voltage and current on a GST line cell (during pulse) at 300 K (a), *I-V* characteristics using PA at 300 K after amorphization at 76, 972 and 2163 seconds (b), *I-V* characteristics using PA at 300 K after annealing at 470 K for 15 min. (c), and resistance change as a function of time (c). The device is amorphized and then crystallized by annealing at 470 K for TEM analysis.

Electrical characteristics show linear *I-V* characteristics and low resistance state (crystalline) is achieved (with ~20 kΩ final resistance) by annealing (Figure 3.41b-d).

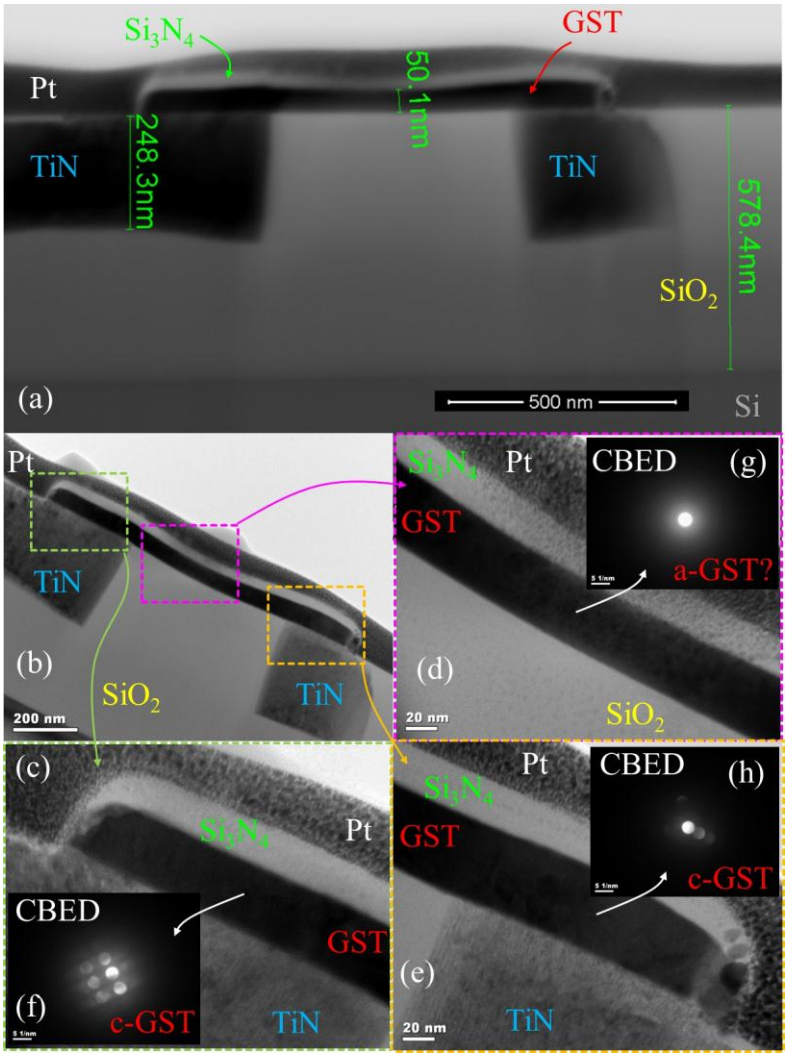


Figure 3.42. TEM images of an amorphized and crystallized (annealed at 470 K for 15 min.) device (line section dimensions: *L*: ~320 nm, *W*: ~100 nm, *t*: ~50nm) (a-e), Converged beam electron diffraction patterns from the pointed areas (f-h). (TEM and CBED images are taken by Roger Ristau in IMS at UConn).

Converged beam electron diffraction patterns confirm that the material is crystalline on the sides with large crystal grains shown in Figure 3.42c,e,f,h. The center part of the structure shows an amorphous diffraction pattern (Figure 3.42d,g). There is some Pt deposited around the center of the device during the FIB process. Also, the second device may not have been cut from the center, hence there might not be enough

GST remaining to observe a crystalline diffraction pattern since the other side of the cross sectioned area may contain some Si_3N_4 capping material. Ion milling and thinning process may change the crystal structures during FIB process. Hence, this could be another reason amorphous diffraction patterns are observed around the center part of the device.

Although this TEM analysis is not conclusive, we have observed crystal grains in amorphous GST with varying sizes (~1-20 nm) [5, 18, 94, 95]. Large crystal grains (> 20 nm) are observed around the side of the sample which is annealed at 470 K for 15 min. Device dimensions are also confirmed with the TEM analysis.

3.12 Hall measurements

Knowledge of transport properties such as carrier density and mobility of GST is also important for the understanding of PCM device operation. Hall measurement can be used to determine carrier type, density and mobility of semiconductors [42]. We performed hall measurements using van der Pauw method on 50 nm thick GST thin film samples annealed at various temperatures and times using an HP 4145B semiconductor parameter analyzer and a measurement apparatus with large brass contacts (Figure 3.43).

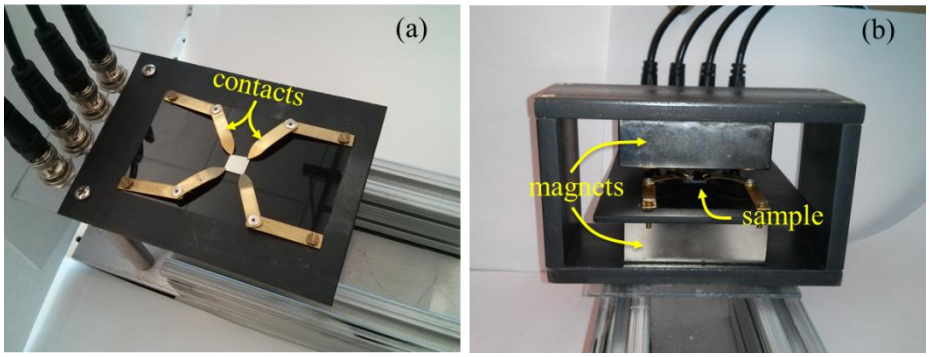


Figure 3.43. Hall measurement apparatus consisting of a sample holder with 4-electrical contacts (a) and a removable pair of strong magnets (b) to provide "up" and "down" magnetic field configurations (B ~0.7 T) (b). (The Hall measurement setup was built by Lhacene Adnane).

The first step of this method is calculating the resistivity of the sample using applied currents between two neighboring contacts and measured voltage differences between the other two contacts. This is repeated for 2 orientations (Figure 3.44) (Equation 3.12). Linear *I-V* characteristics observed suggesting good electrical contacts (Figure 3.45).

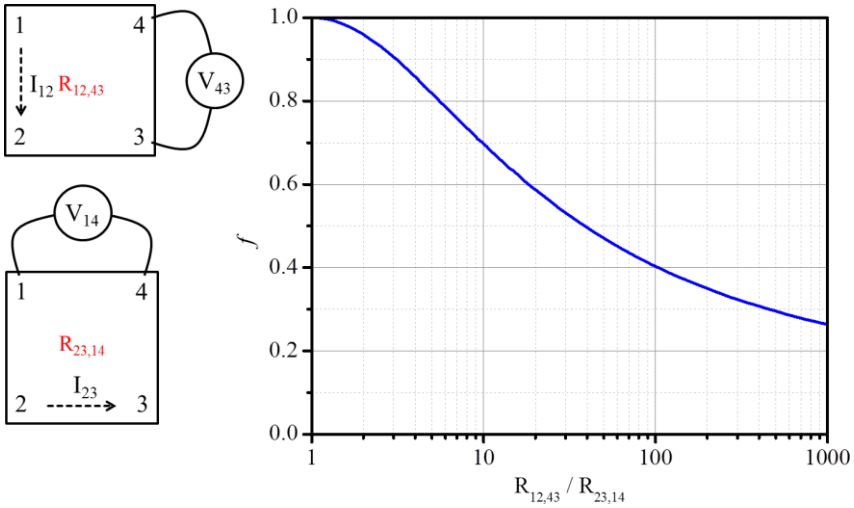


Figure 3.44. Schematic illustration of resistivity calculation using the van der Pauw method (left) and geometry correction factor (f) as a function of the measured resistance ratio (right) [42].

$$R_{12,43} = \frac{V_{43}}{I_{12}} \tag{3.10}$$

$$R_{23,14} = \frac{V_{14}}{I_{23}} \tag{3.11}$$

$$\rho = f \frac{\pi t}{\ln 2} \frac{(R_{12,43} + R_{23,14})}{2} \tag{3.12}$$

where, *f*: geometry correction factor, *t*: sample thickness.

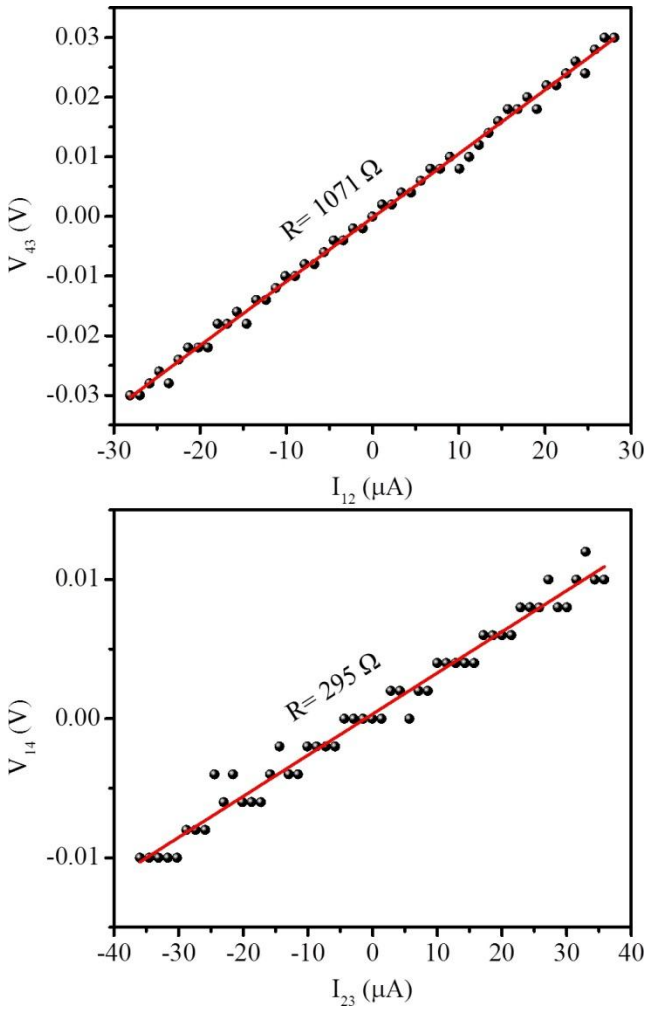


Figure 3.45. Example van der Pauw *I-V* characteristics for resistance calculations for a sample annealed at *T*= 550 K for 2000 s.

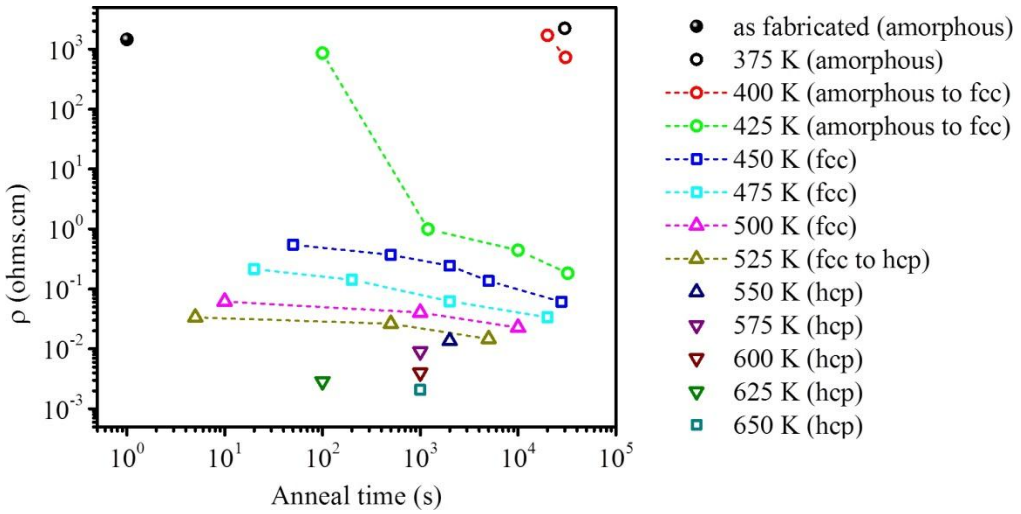


Figure 3.46. Electrical resistivities of the GST thin films annealed at various temperatures and times.

I-V characteristics of amorphous and crystalline GST thin films are obtained using an applied current and measured voltage difference under strong magnetic field (B ~0.7 T) for "up" and "down" magnetic field directions (Figure 3.47).

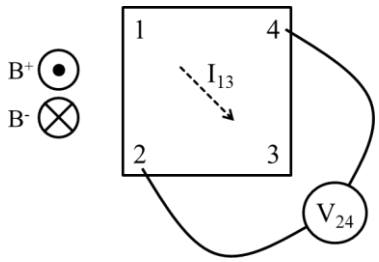


Figure 3.47. Schematic illustration of Hall voltage measurement using the van der Pauw method.

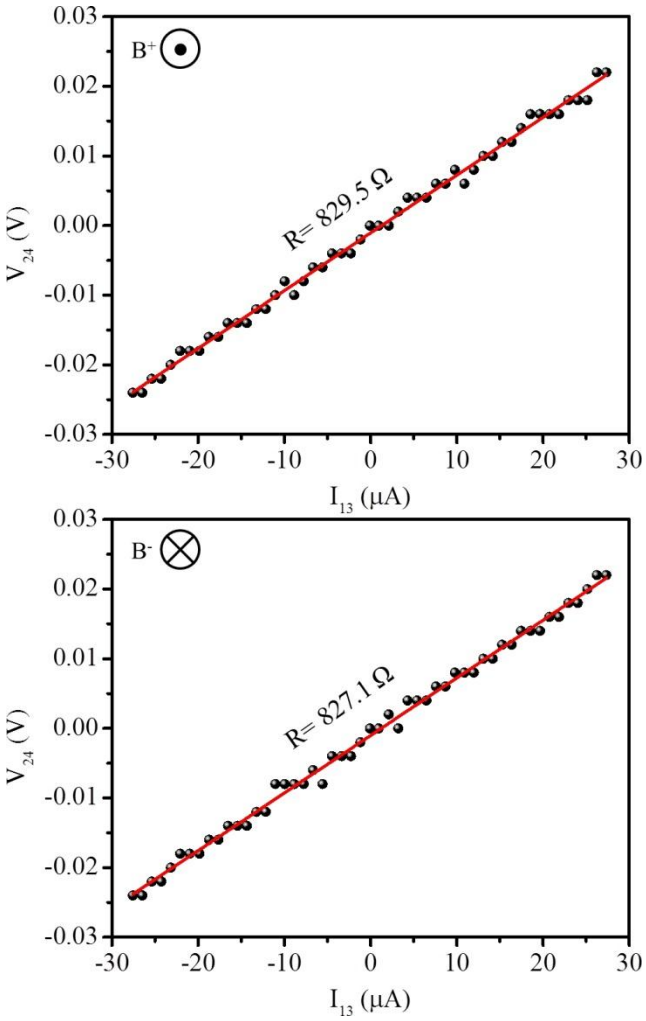


Figure 3.48. Example van der Pauw *I-V* characteristics for resistance calculations for "up" and "down" magnetic field directions for a sample annealed at *T*= 550 K for 2000 s to determine the Hall voltage V_H.

$$\frac{V_H}{I} = \frac{R^{B^+} - R^{B^-}}{2} \tag{3.13}$$

Slopes of the linear regression of *I-V* characteristics are used for resistance calculations. Resistance values used in Hall Voltage calculations are from the average of 3 repeated *I-V* measurements. The carrier density and mobility are calculated using Equations 3.14 and 3.15.

$$n, p = \frac{B \times I}{|V_H| \times e \times t} \tag{3.14}$$

$$\mu = \frac{|V_H| \times t}{I \times B \times \rho} \tag{3.15}$$

where, B is the magnetic field, e is electron charge, t is the thickness, and ρ is the resistivity of the sample. Results show that the hole density increases from ~10^{14} cm^{-3} for amorphous phase to ~10^{19} for crystalline (fcc) phase and ~10^{20} cm^{-3} for crystalline (hcp) phase GST (Figure 3.49a) and Hall mobility fluctuates between ~1 to 300 $cm^2/V.s$ at room temperature (Figure 3.49b) [63]. Each data point comes from a single measurement performed on a single sample. However, despite the good linear *I-V* characteristics obtained from R_B^+ and R_B^- for each sample, even the crystalline samples show very large variations in carrier concentration and mobility. There is no observed trend with anneal temperature and time. The reasons for those large variations are not clear at this point. Difficulty in performing these measurements and an anomalous Hall effect has been reported for amorphous GST in the literature [106, 107].

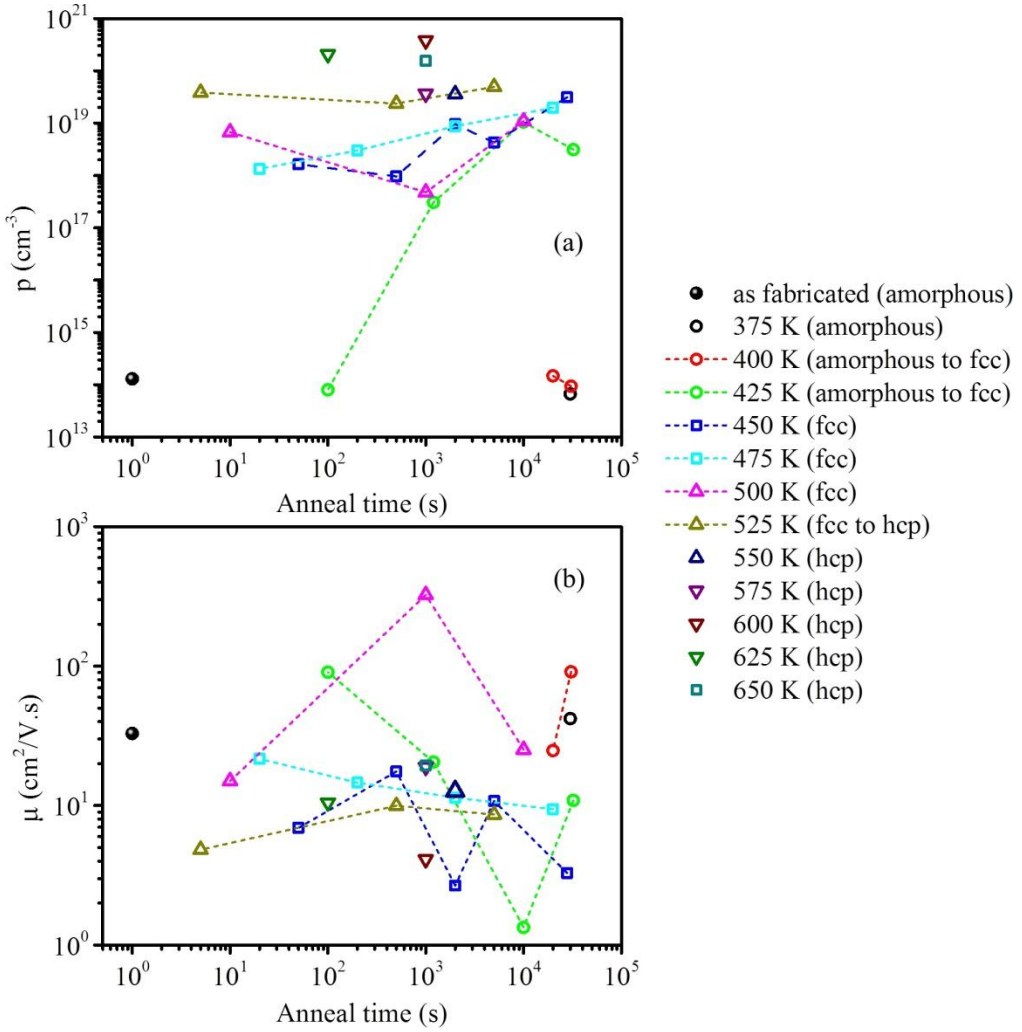


Figure 3.49. Carrier concentrations (a), and Hall mobilities (b) of the GST thin films annealed at various temperatures and times. Unexpectedly no consistent trend for carrier concentration and mobility as a function of anneal temperature and time was observed from these measurements.

4. Conclusion

Phase change memory (PCM) device operation strongly depends on the electrical, thermal and electrothermal properties of the materials used as well as the device structure. The phase change material properties are the most critical and have to be characterized for all phases experienced during device operation. Characterization of the liquid phase and the metastable amorphous and fcc phases requires high-speed electrical techniques as described in this work.

The electrothermal simulations of GST bridge structures using the measured parameters are in good agreement with the experimental reports on asymmetric heating of lateral phase change structures where melting has been consistently observed at the higher potential end. While these computational studies verify that the asymmetry in melting is driven by Thomson heat, the overall impact on lateral structures is not as significant since the active region is away from the contacts and the resistance contrast does not change significantly. The overall thermoelectric effects is less on lateral structures compared to mushroom and confined cells, which one of their electrodes are in contact with the active region.

The highly sensitive, high-speed characterization technique developed to characterize the metastable phases can be used in a wide temperature range at the device level and does not rely on the ramp-rate of a hot-chuck. The samples are kept at the desired measurement temperature hence the devices can be rapidly brought down to the measurement temperature after melting. Using the described waveforms, electrical

resistivity of GST in the crystalline state (before the pulse), liquid state (during the pulse) and metastable amorphous and fcc states (after the pulse) are directly measured for temperatures between 300 K and 675 K in a single measurement. The resistivity of liquid $Ge_2Sb_2Te_5$ (GST) at the device level was measured to be ~0.26 mΩ.cm, close to the values reported for bulk GST. The metastable amorphous and fcc resistivities are found to follow exponentially decreasing functions of temperature that are significantly higher compared to values obtained from typical slow *R-T* measurements. Three distinct activation energies are obtained for the 300-675 K temperature range, suggesting different carrier activation processes at various temperature ranges. Some information on the crystallization dynamics and resistance drift in the amorphous phase is also obtained from the same measurements. Crystallization times are extracted by monitoring the resistance over short duration (~2 ms) after amorphization at each chuck temperature using AC high-speed measurements and over long duration (~3-30 min) using a DC baseline voltage and a DAQ card. Resistance drift in amorphous phase is observed at various temperatures (~ 300-500 K) in short (~2 ms) and very long time (~13 months) scales. The devices kept at room temperature have reached their maximum resistance values and started decreasing at ~4 months after amorphization. The overall results show that the nucleation-growth dynamics play a significant role in both resistance drift and carrier activation in various crystalline states.

5. Appendix

5.1 Details of the layout design

The detailed views of designed structures are shown below.

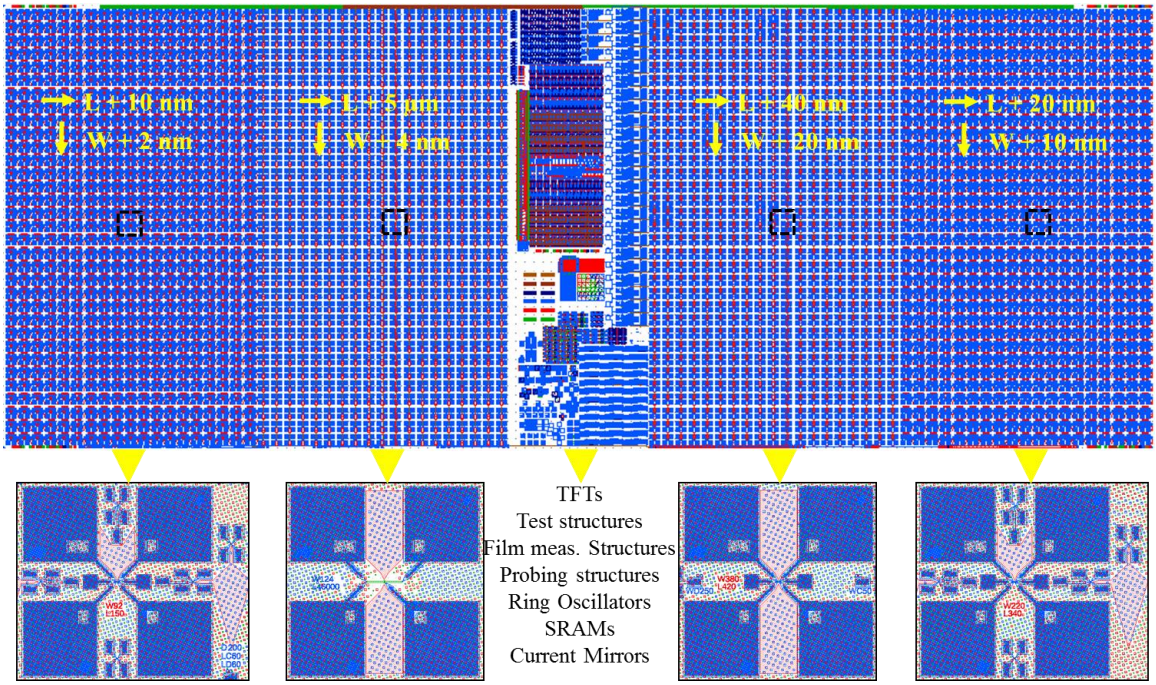


Figure 5.1. Layout of the die and sample devices.

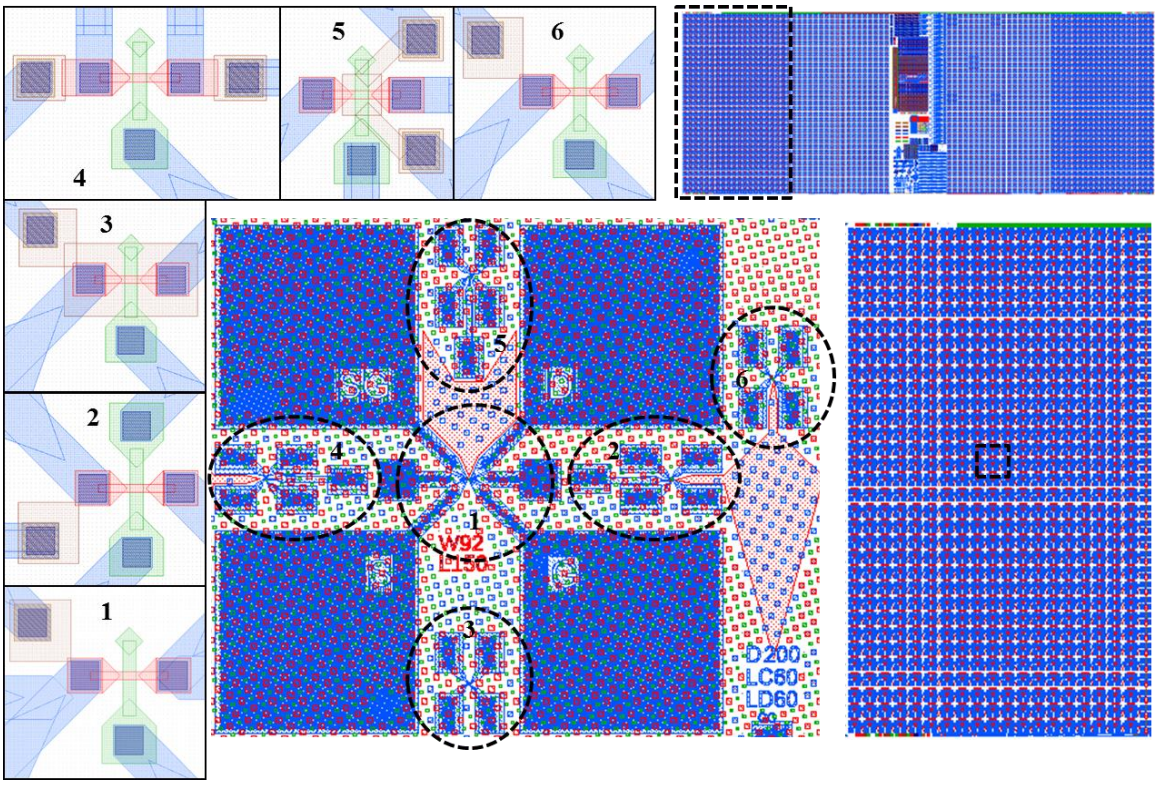


Figure 5.2. Block1 devices with various magnifications.

Table 5.1. Dimensions and number of devices in block1.

	***W* (nm)**	***W* step (nm)**	***L* (nm)**	***L* step (nm)**	**# of device**
1-Main device	60-124	2	60-240	10	627 each
2-Double gate device					
3-SG patch device					
4-Double SG device					
5-Local device					
6-Main device					

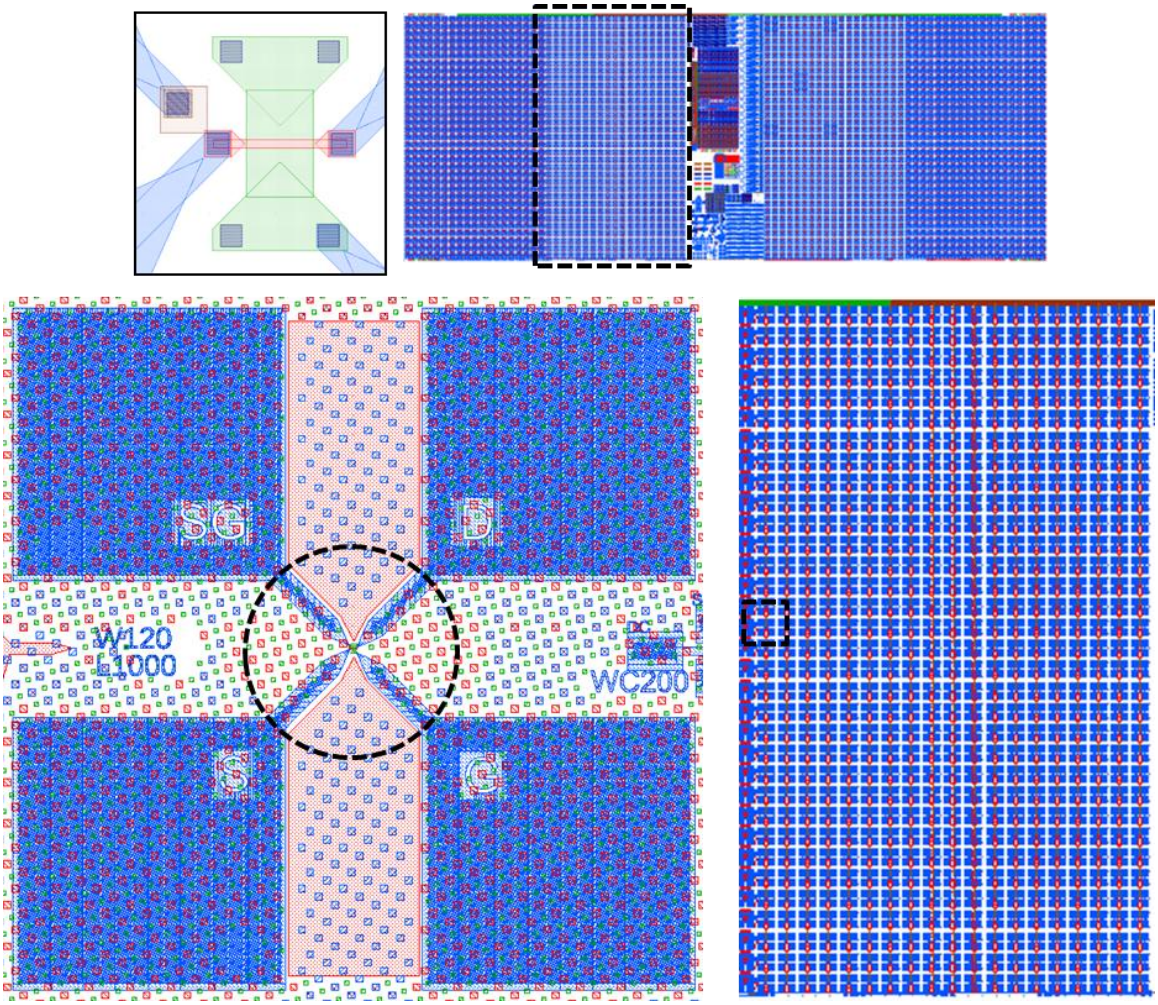


Figure 5.3. Block2 devices top with various magnifications.

Table 5.2. Dimensions and number of devices in block2.

	***W* (nm)**	***W* step (nm)**	***L* (μm)**	***L* step (μm)**	**# of device**
DNA device (long)	60-188	4	1-91	5	627

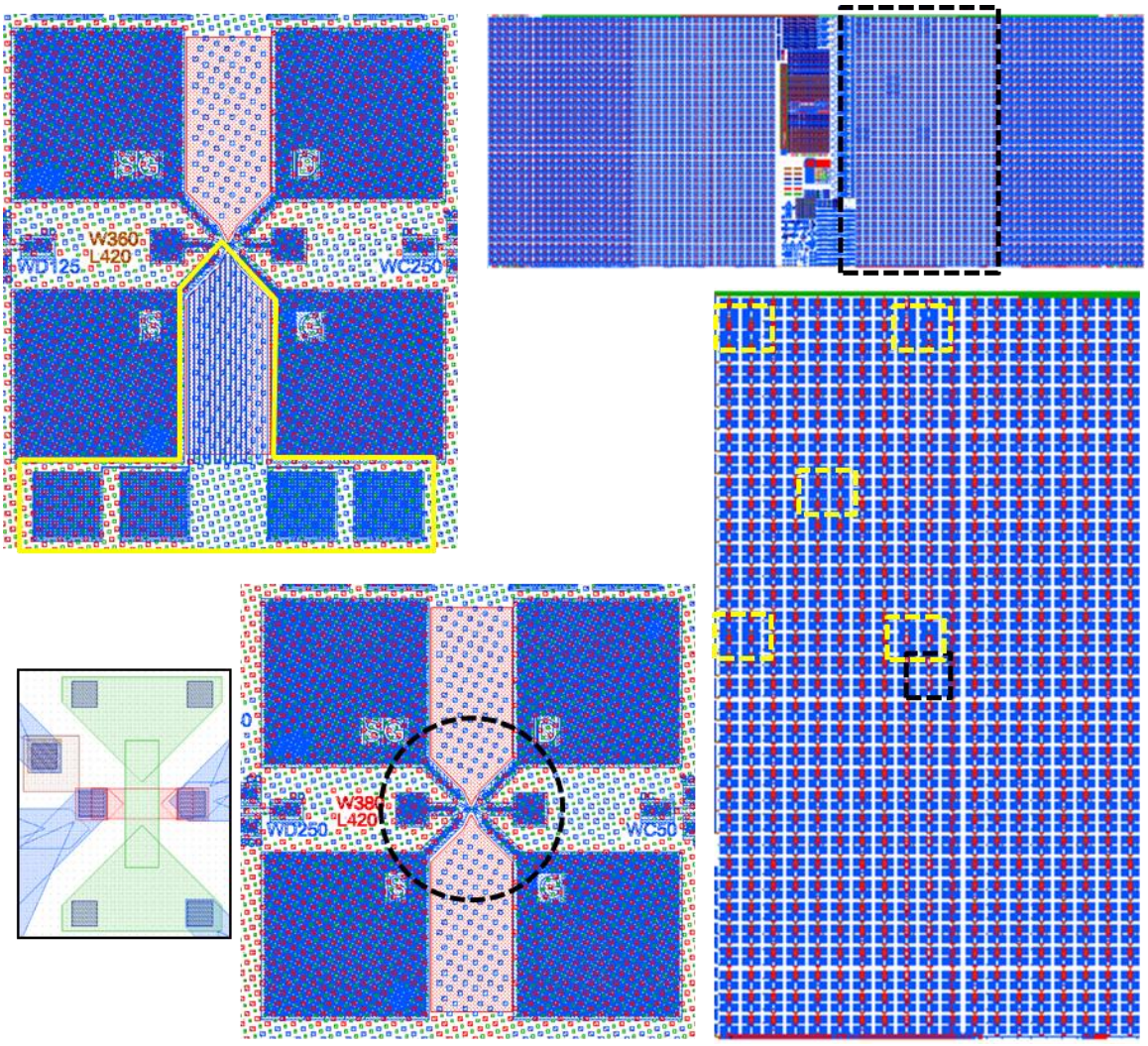


Figure 5.4. Block3 devices top with various magnifications.

Table 5.3. Dimensions and number of devices in block3.

	***W* (nm)**	***W* step (nm)**	***L* (nm)**	***L* step (nm)**	**# of device**
1-DNA device	60-700	20	60-780	40	627
2-Metal heater	300				22

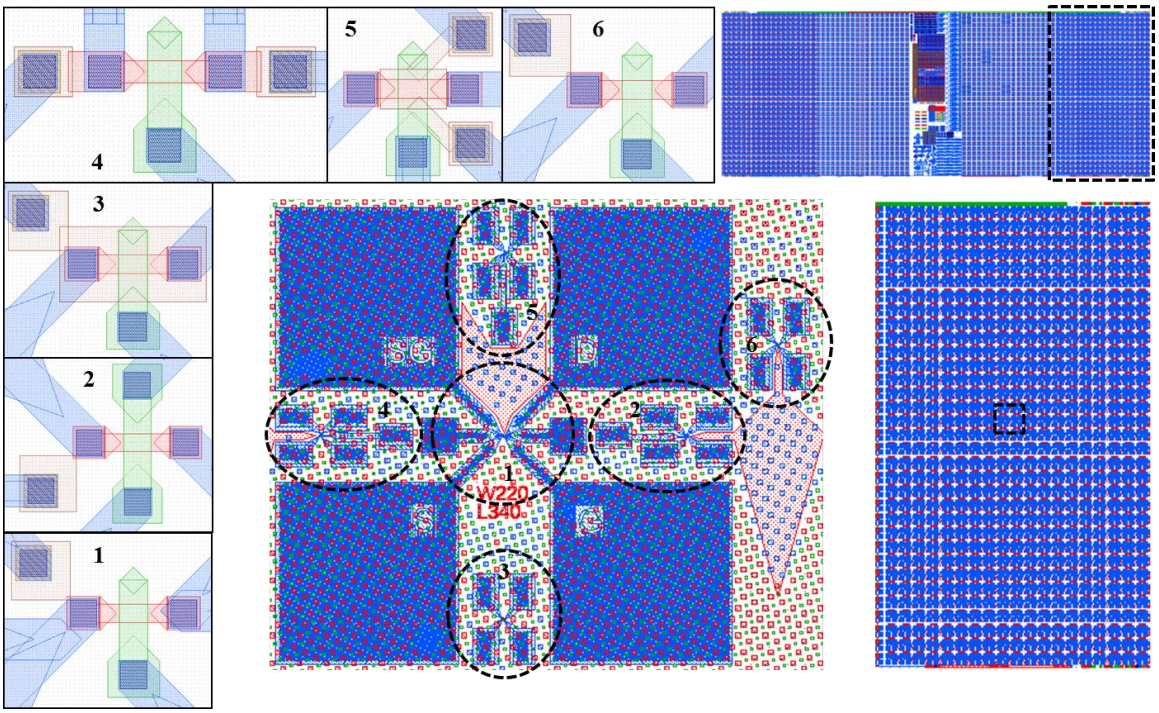


Figure 5.5. Block4 devices top with various magnifications.

Table 5.4. Dimensions and number of devices in block4.

	***W* (nm)**	***W* step (nm)**	***L* (nm)**	***L* step (nm)**	**# of device**
1-Main device	60-380	10	60-420	20	627 each
2-Double gate device					
3-SG patch device					
4-Double SG device					
5-Local device					
6-Main device					

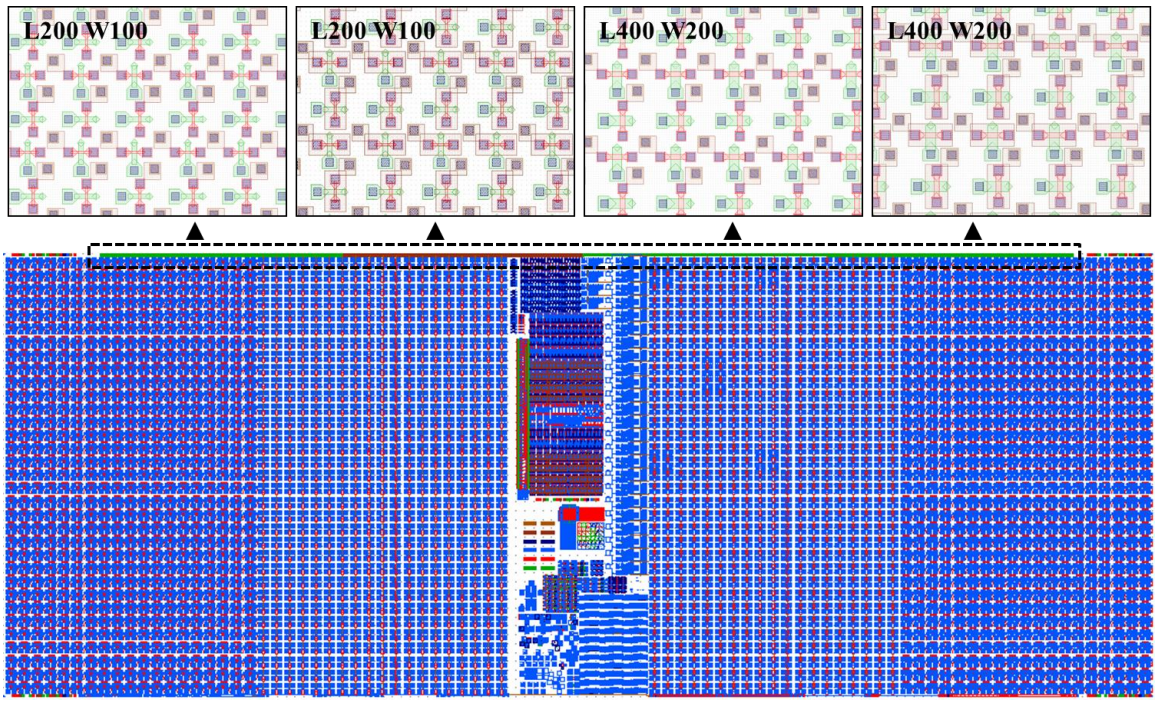


Figure 5.6. Staggered device arrays with zoomed in devices.

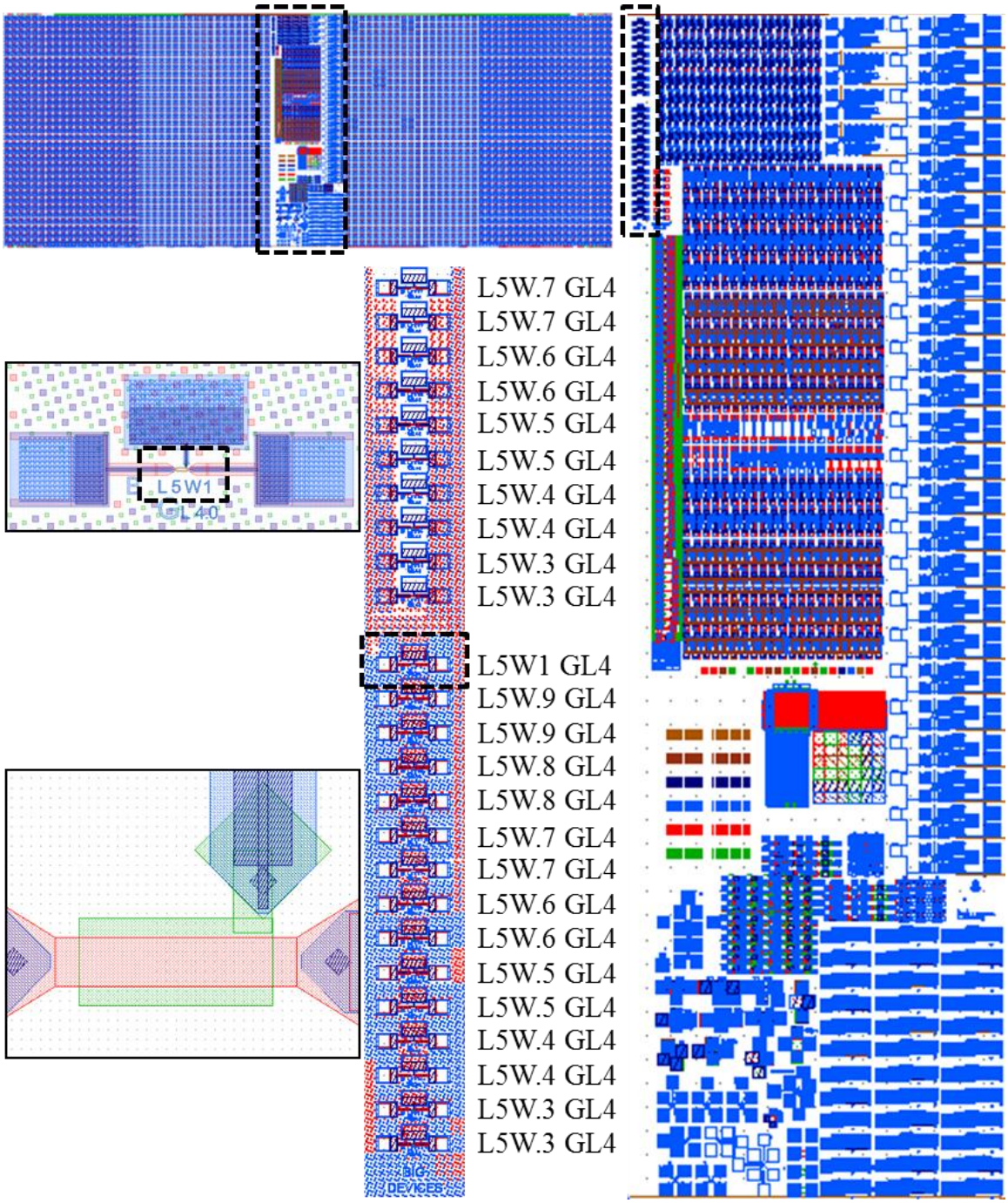


Figure 5.7. Big TFT devices.

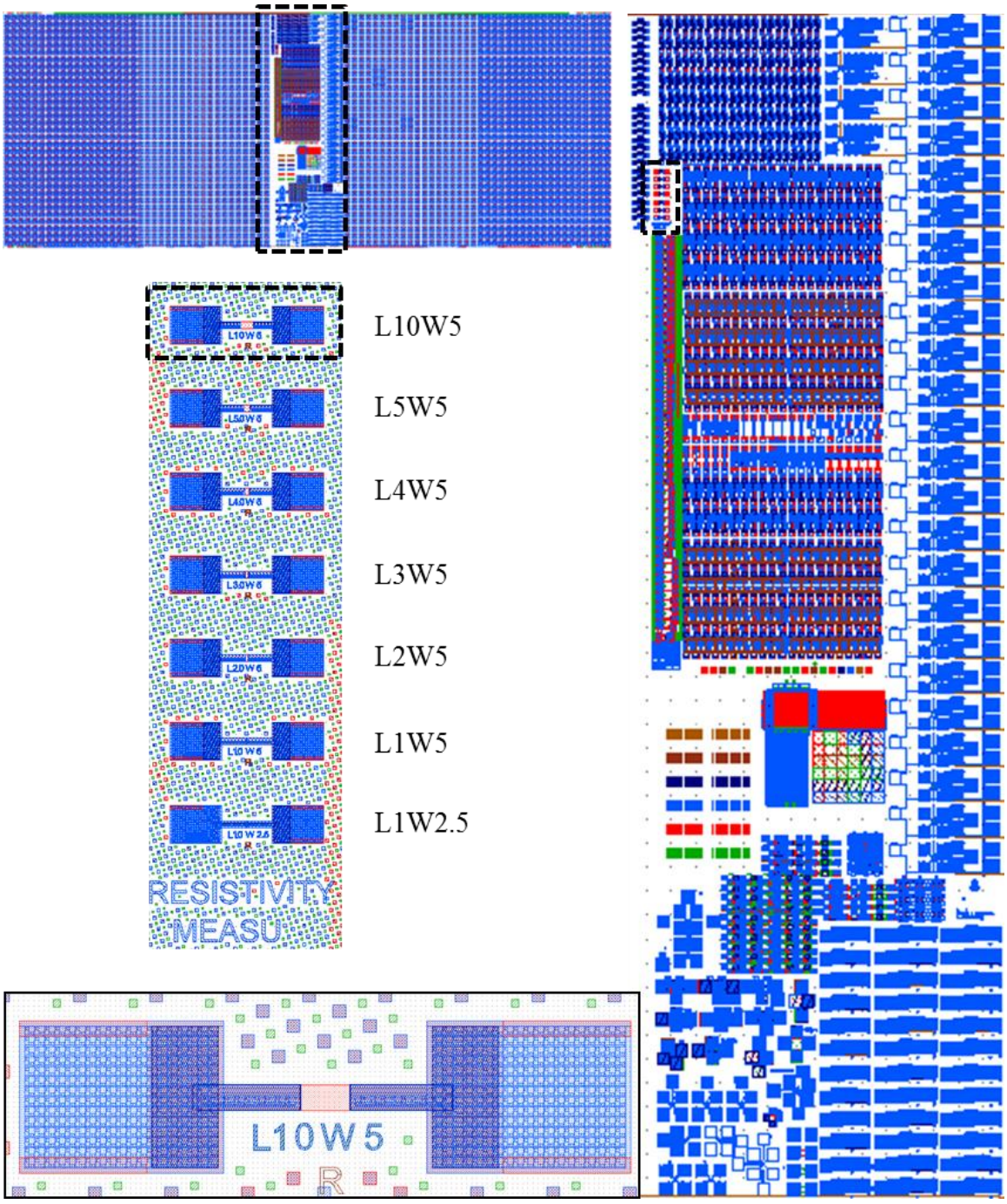


Figure 5.8. Big devices for resistivity measurement.

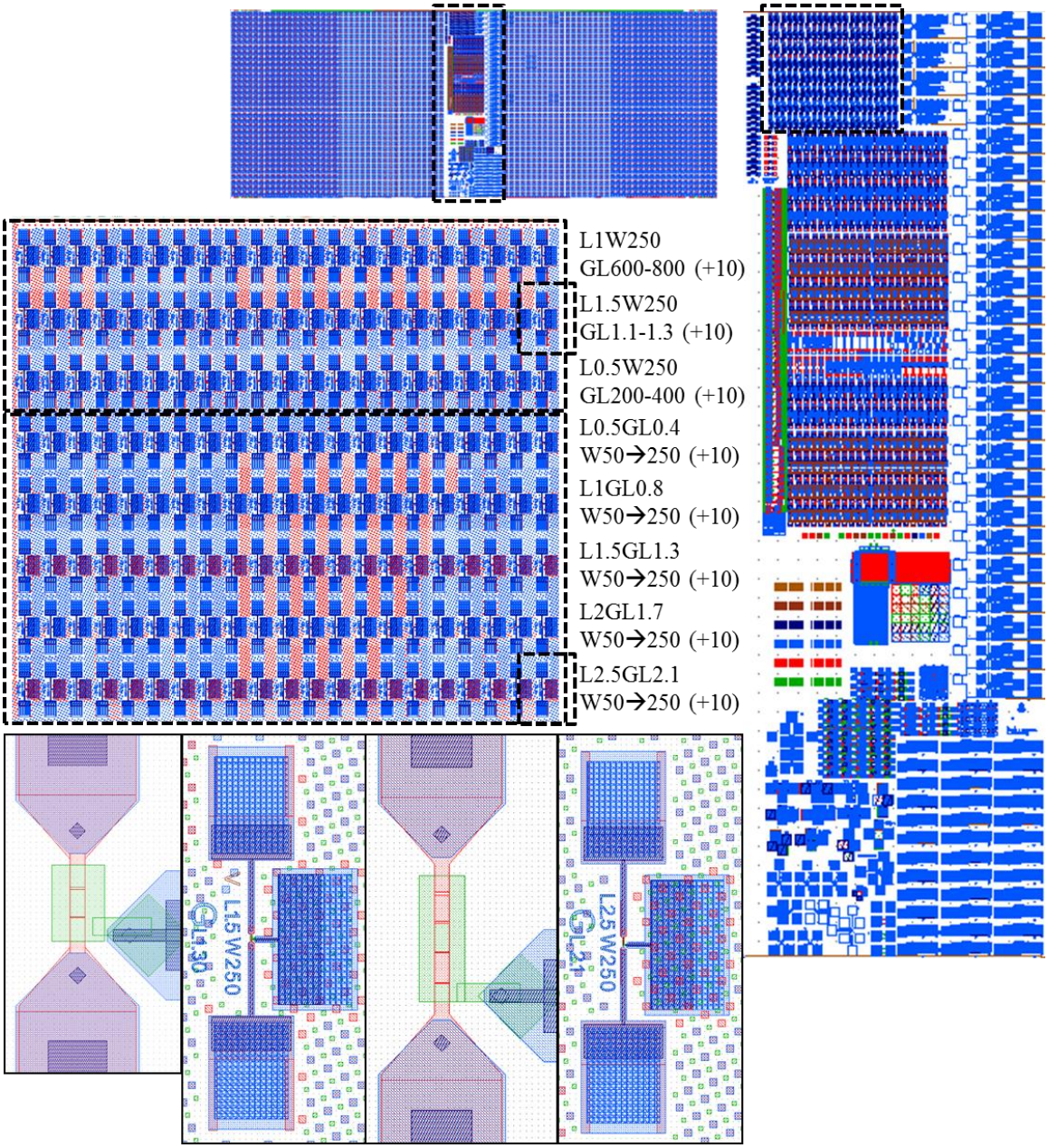


Figure 5.9. Regular TFT arrays.

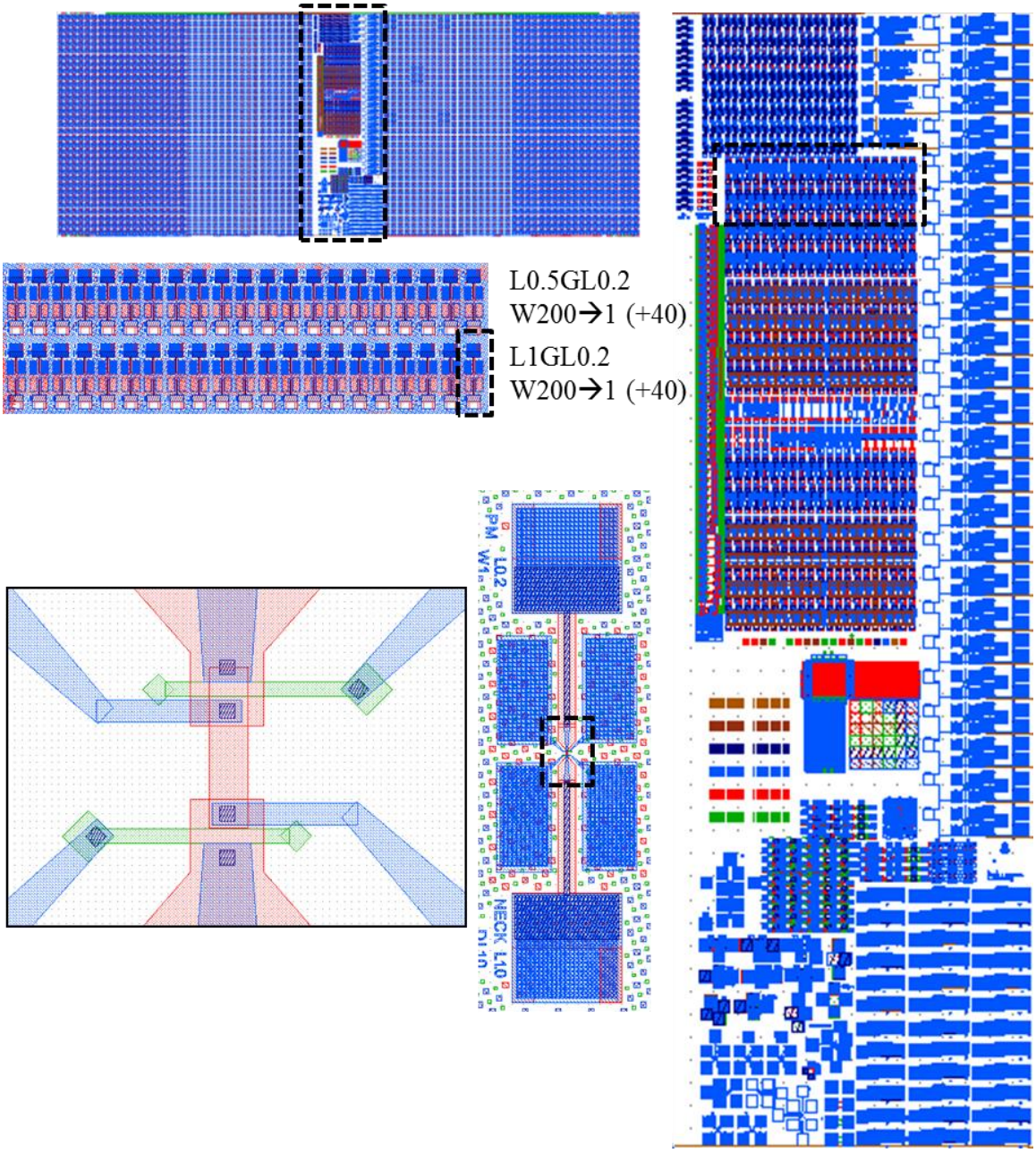


Figure 5.10. Post-modern TFT arrays (1).

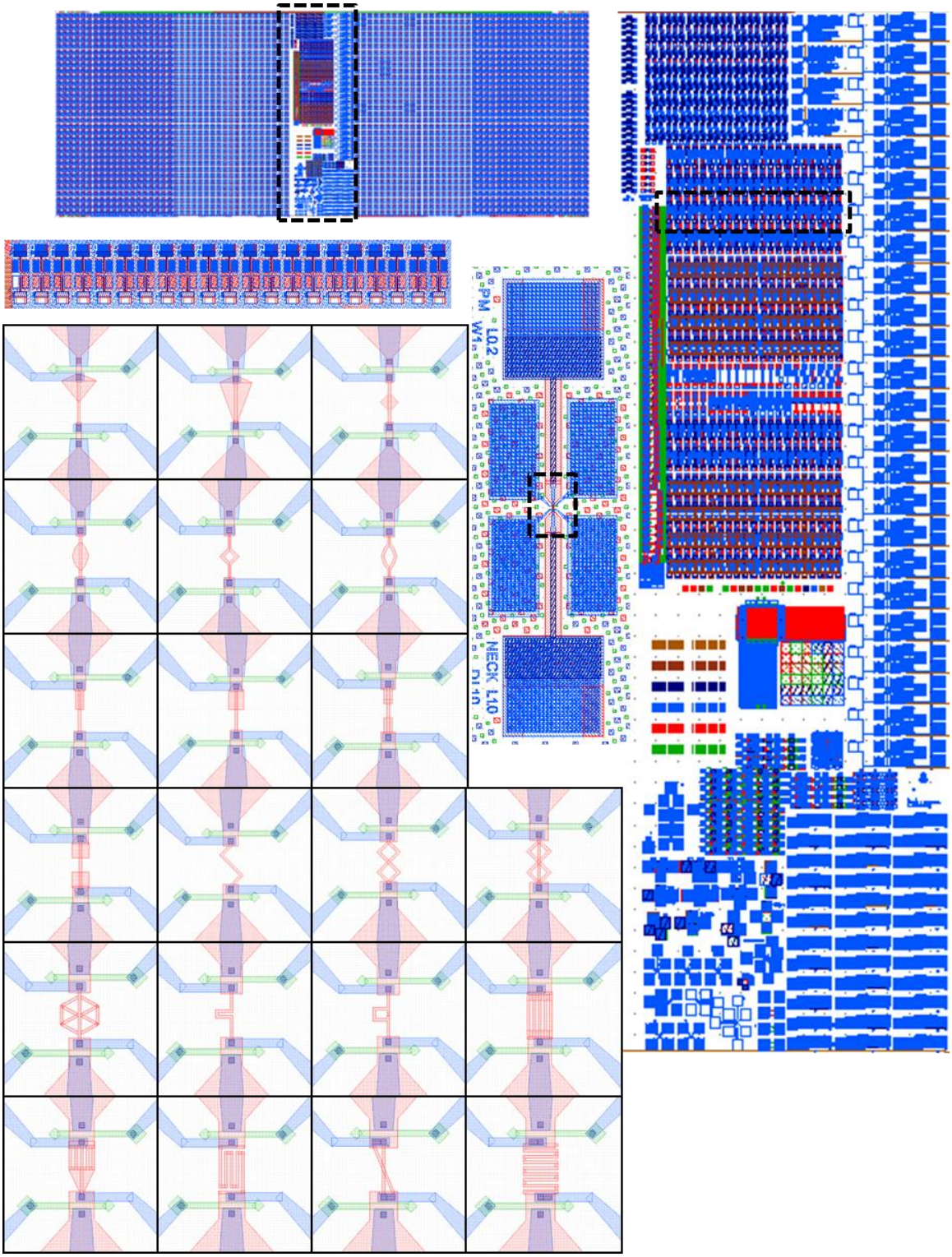


Figure 5.11. Symmetric and asymmetric test structures (1).

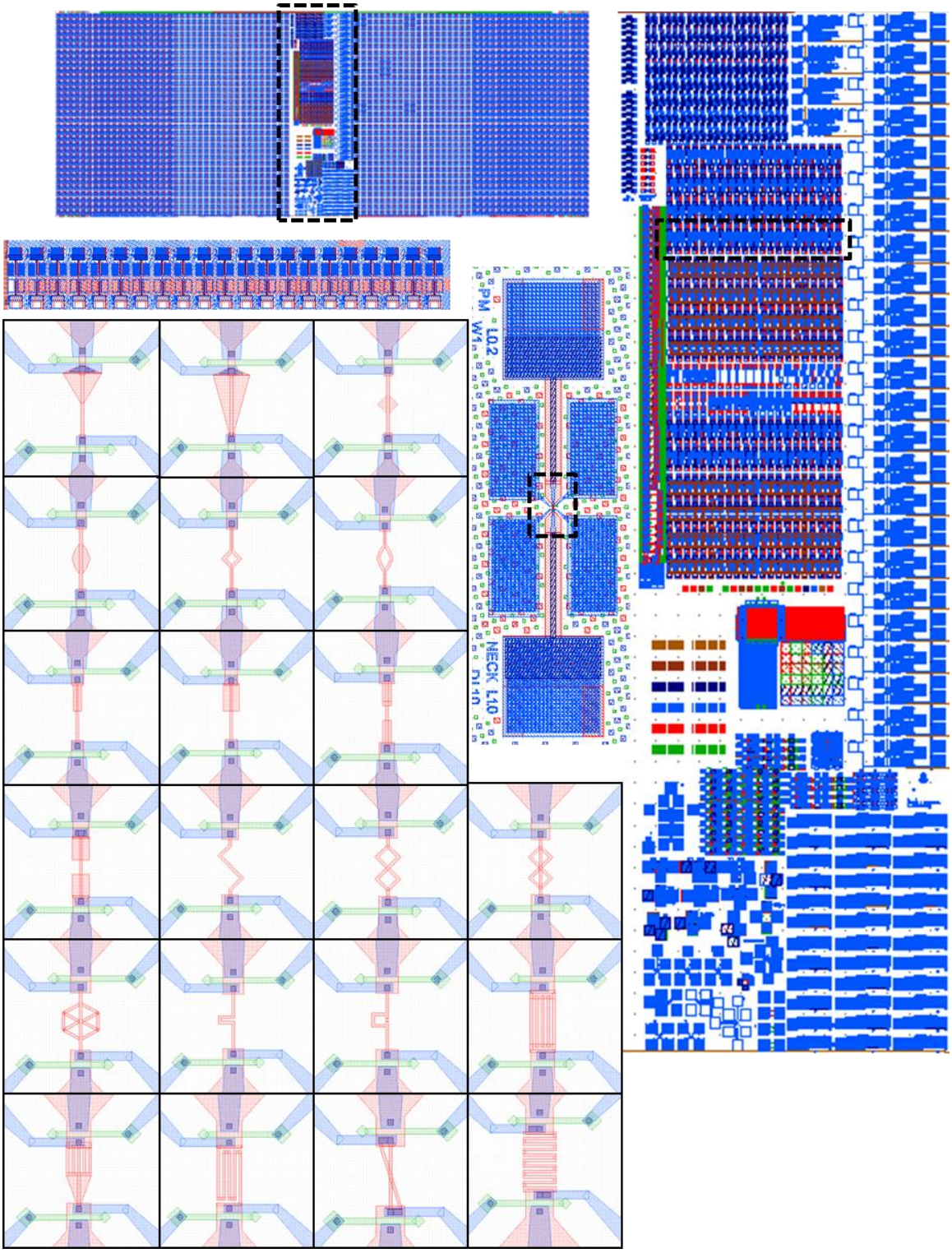


Figure 5.12. Symmetric and asymmetric test structures (2).

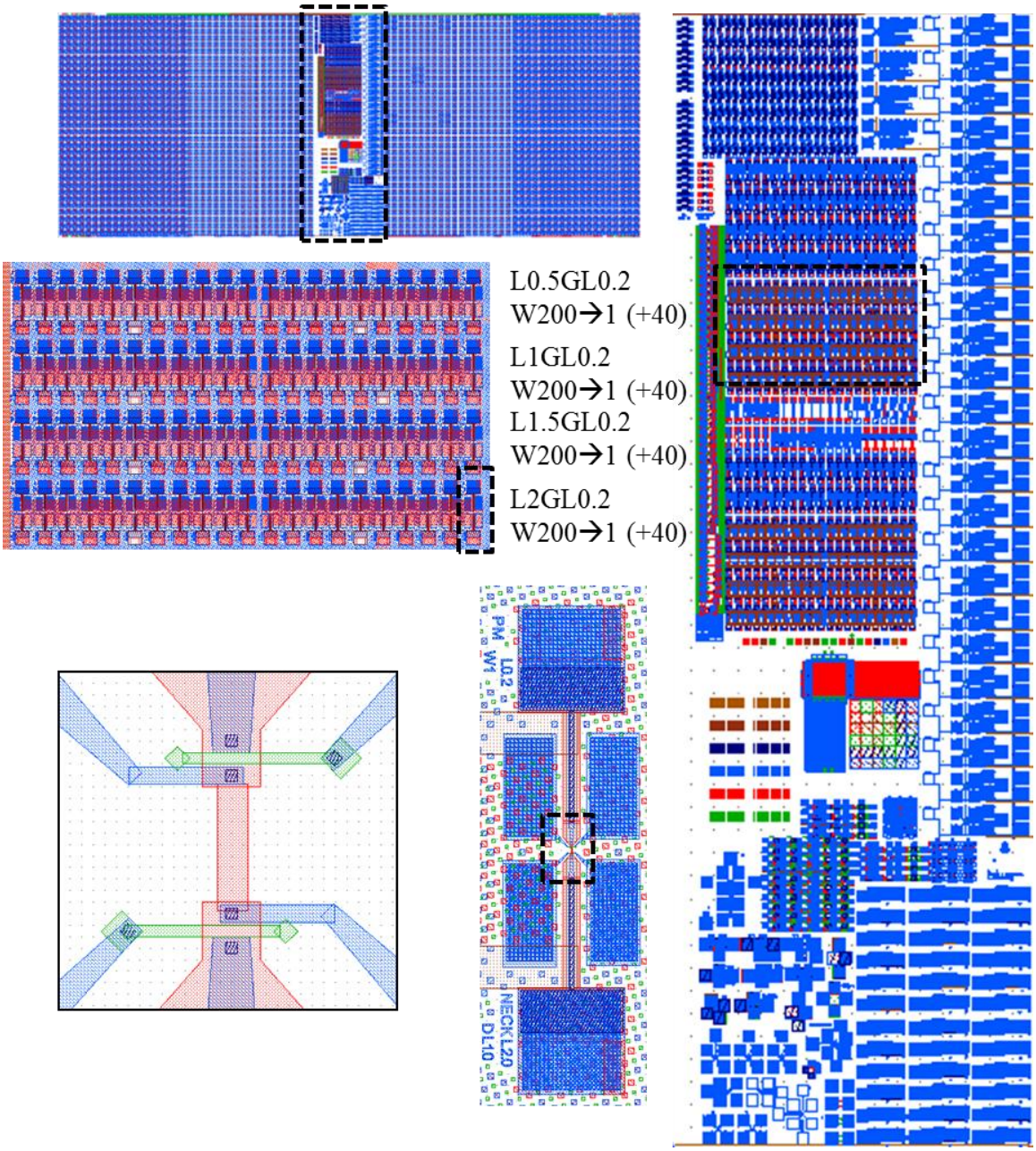


Figure 5.13. Post-modern TFT arrays (2).

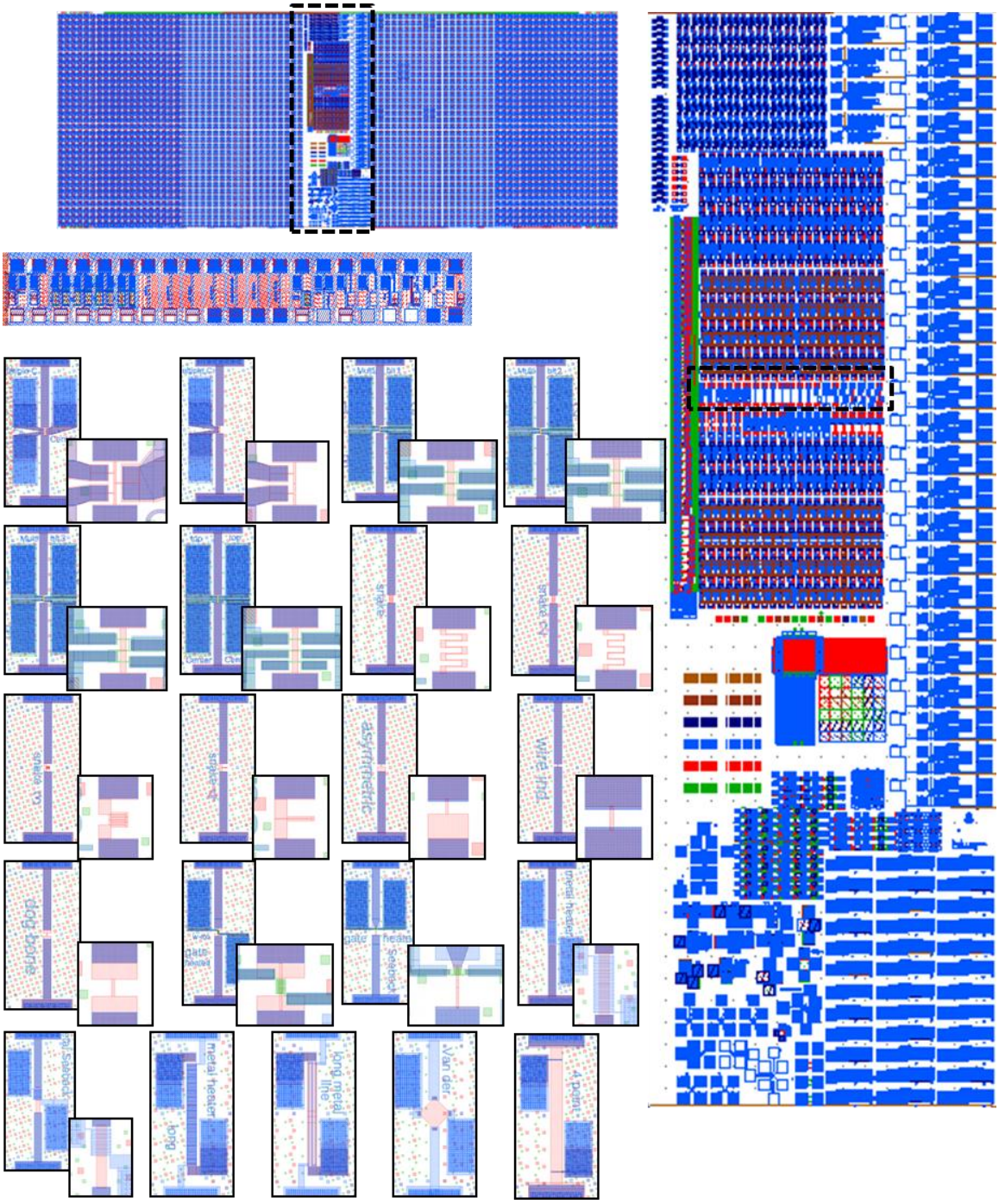


Figure 5.14. Symmetric and asymmetric test structures (3).

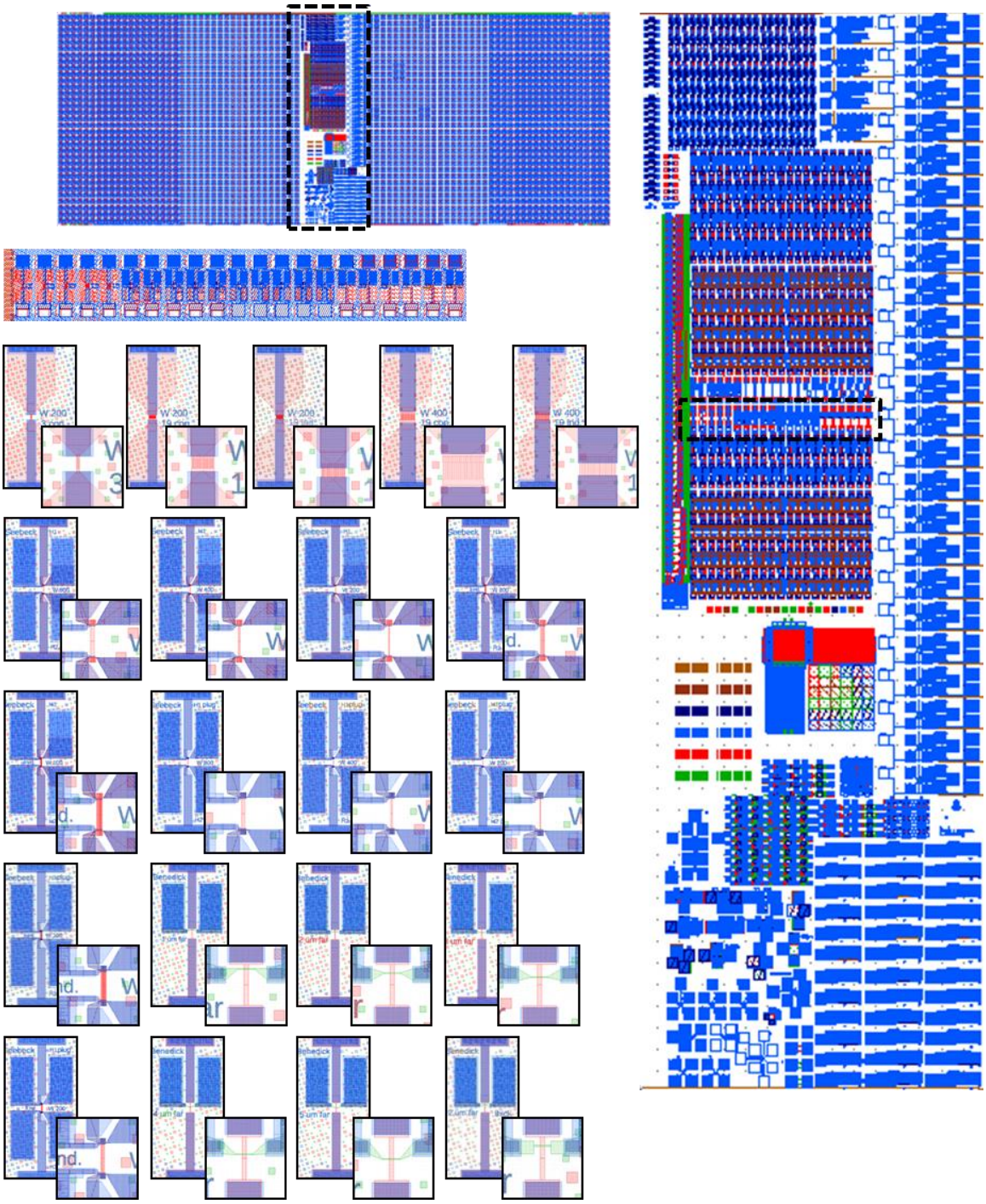


Figure 5.15. Symmetric and asymmetric test structures (4).

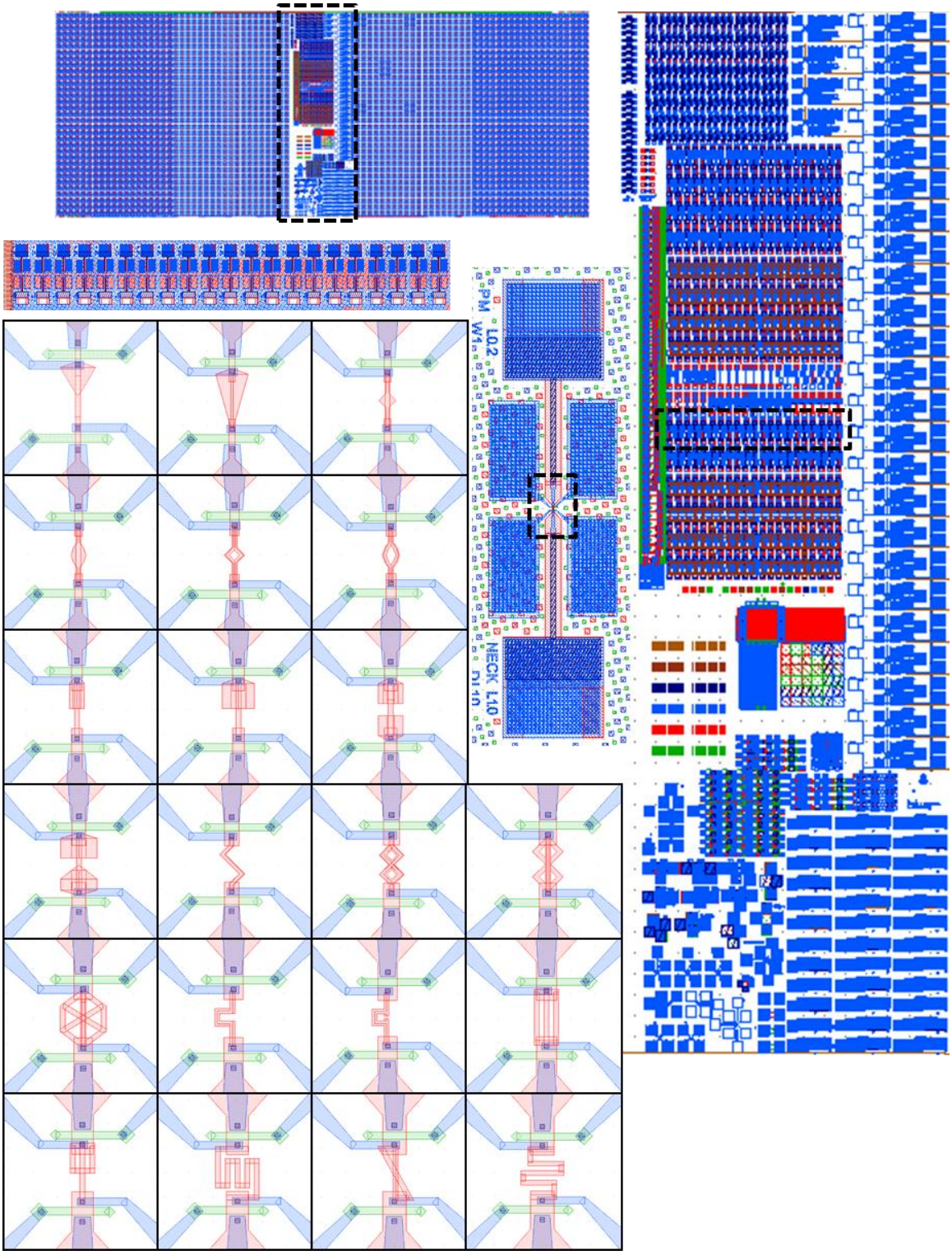


Figure 5.16. Symmetric and asymmetric test structures (5).

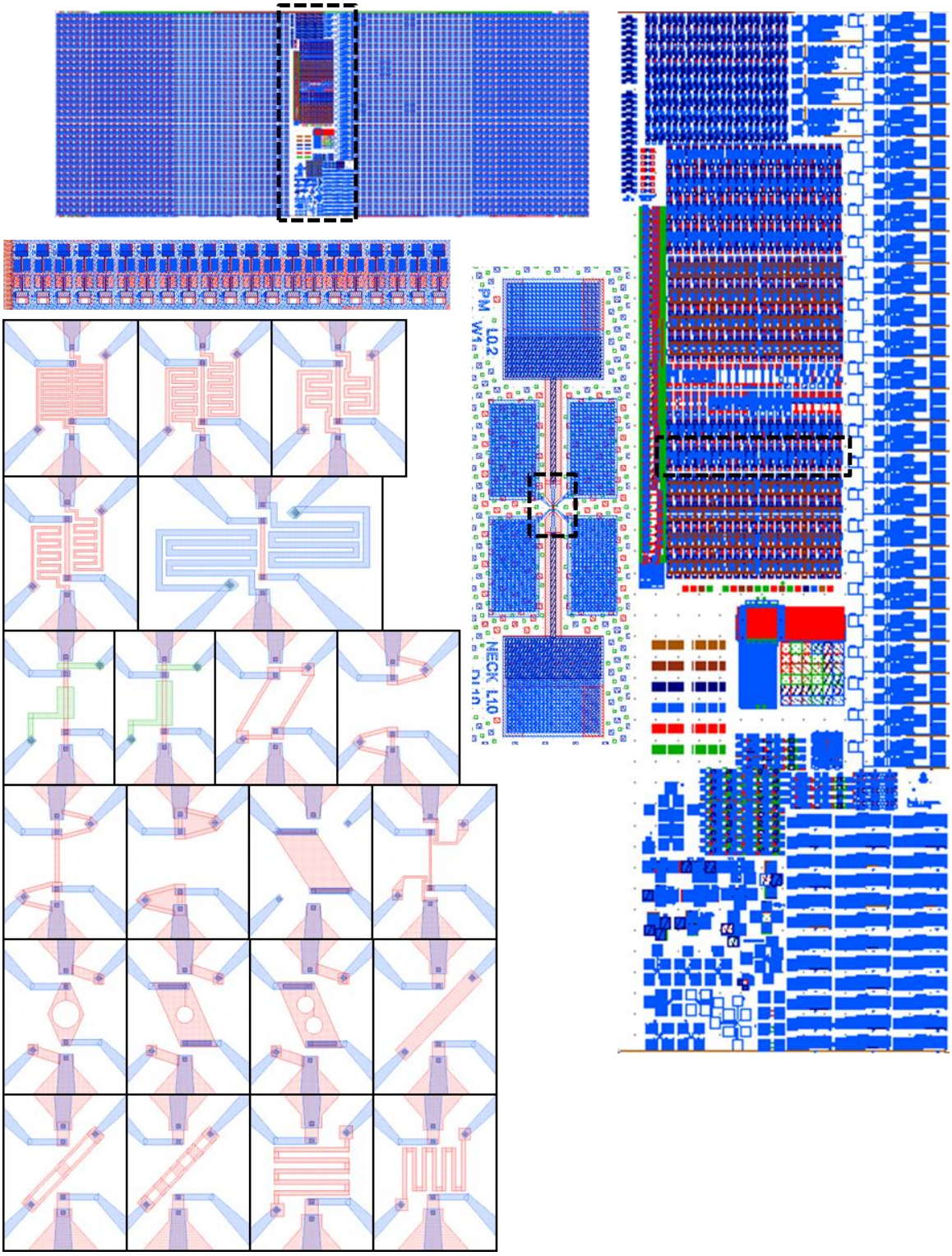


Figure 5.17. Symmetric and asymmetric test structures (6).

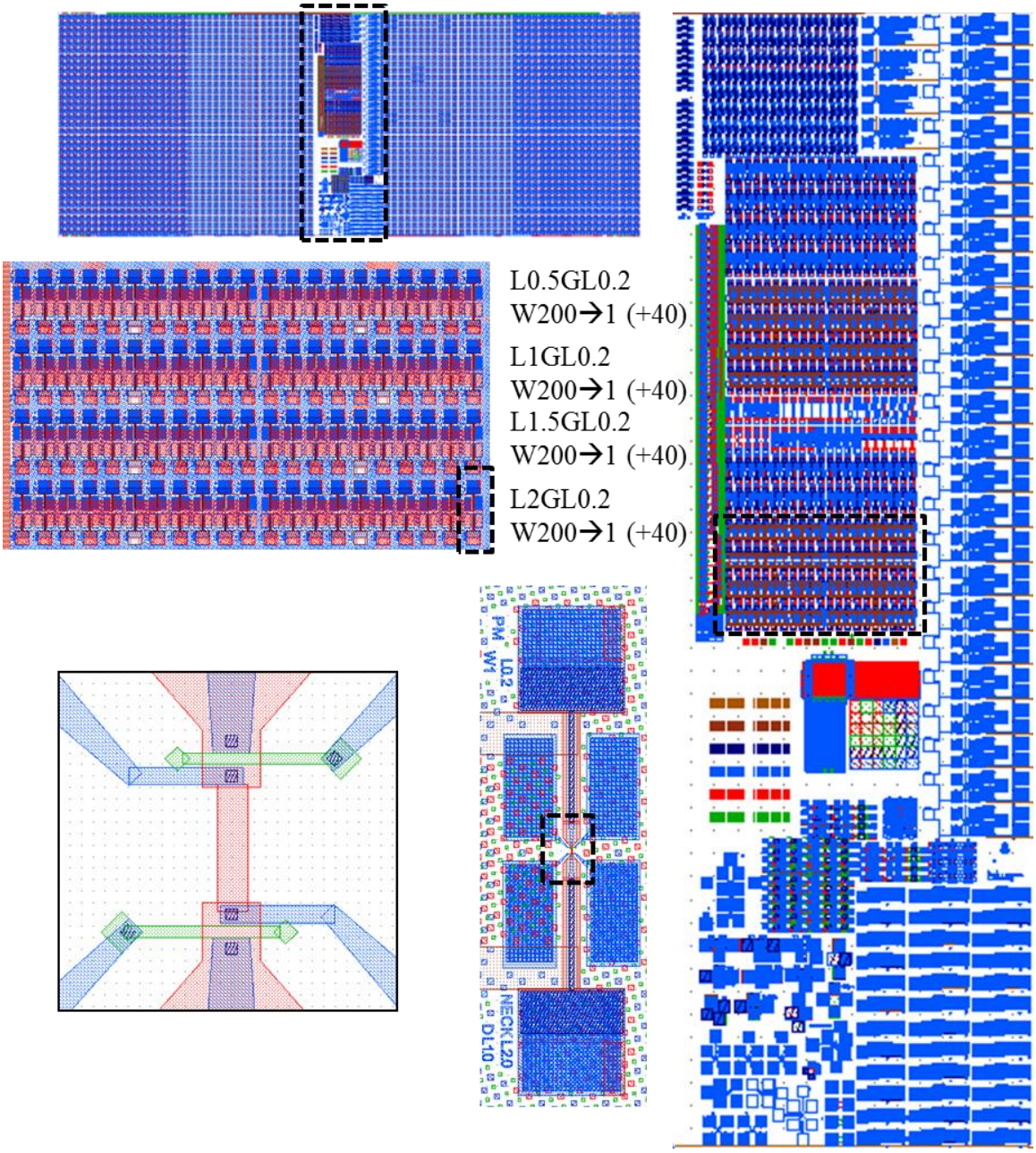


Figure 5.18. Post-modern TFT arrays (3).

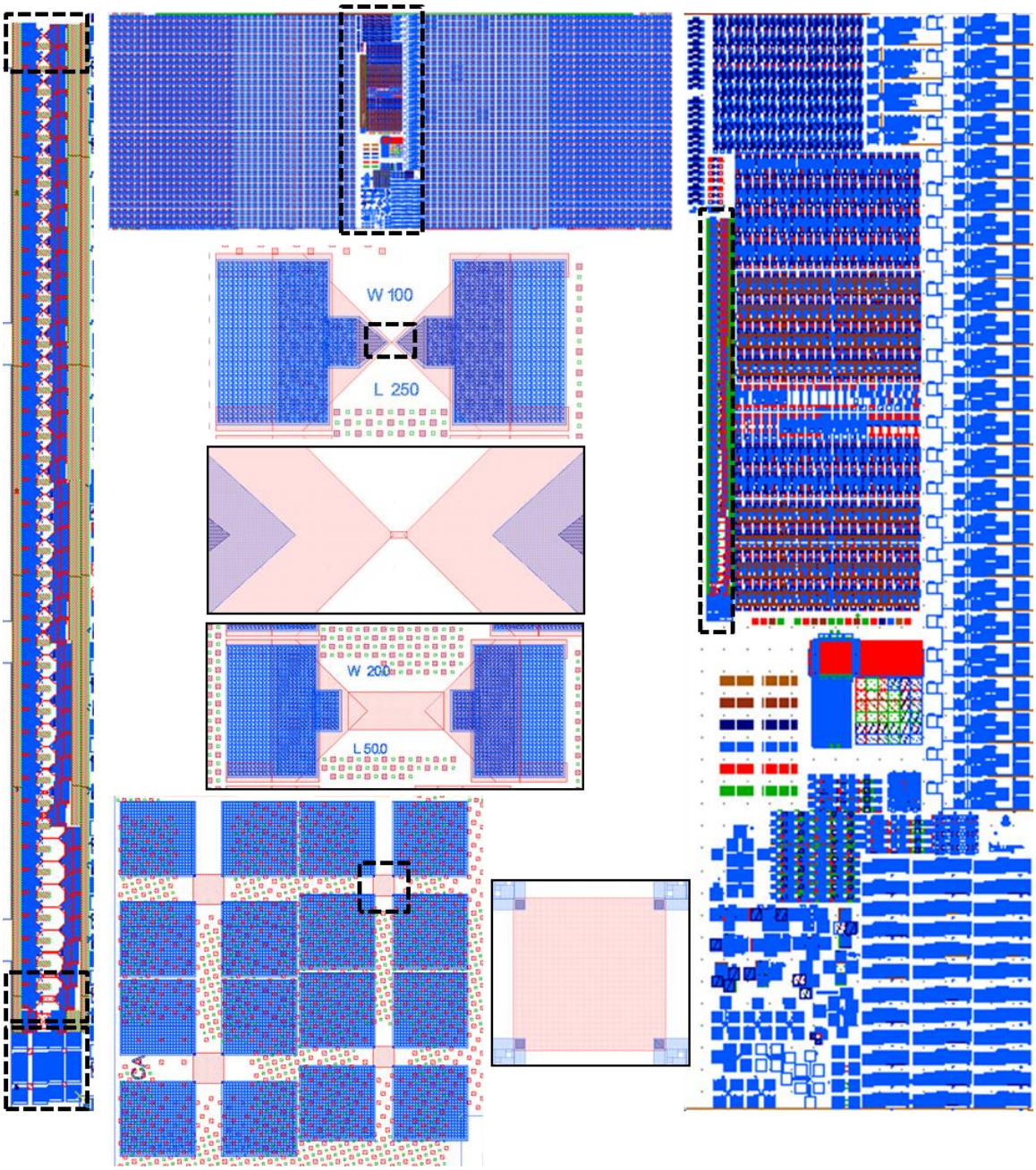


Figure 5.19. Wires with big contacts and Hall measurement structures.

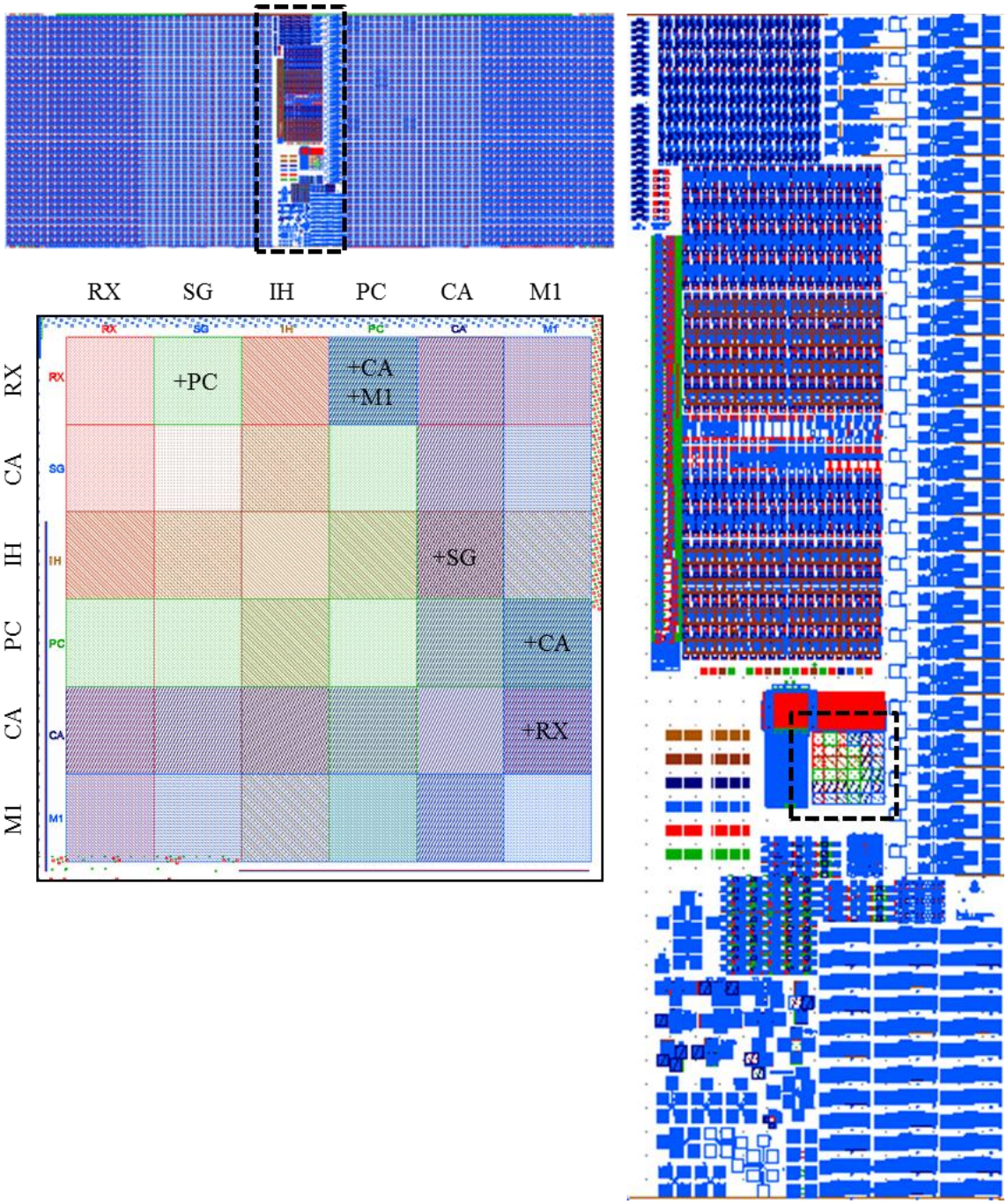


Figure 5.20. Film measurement structures.

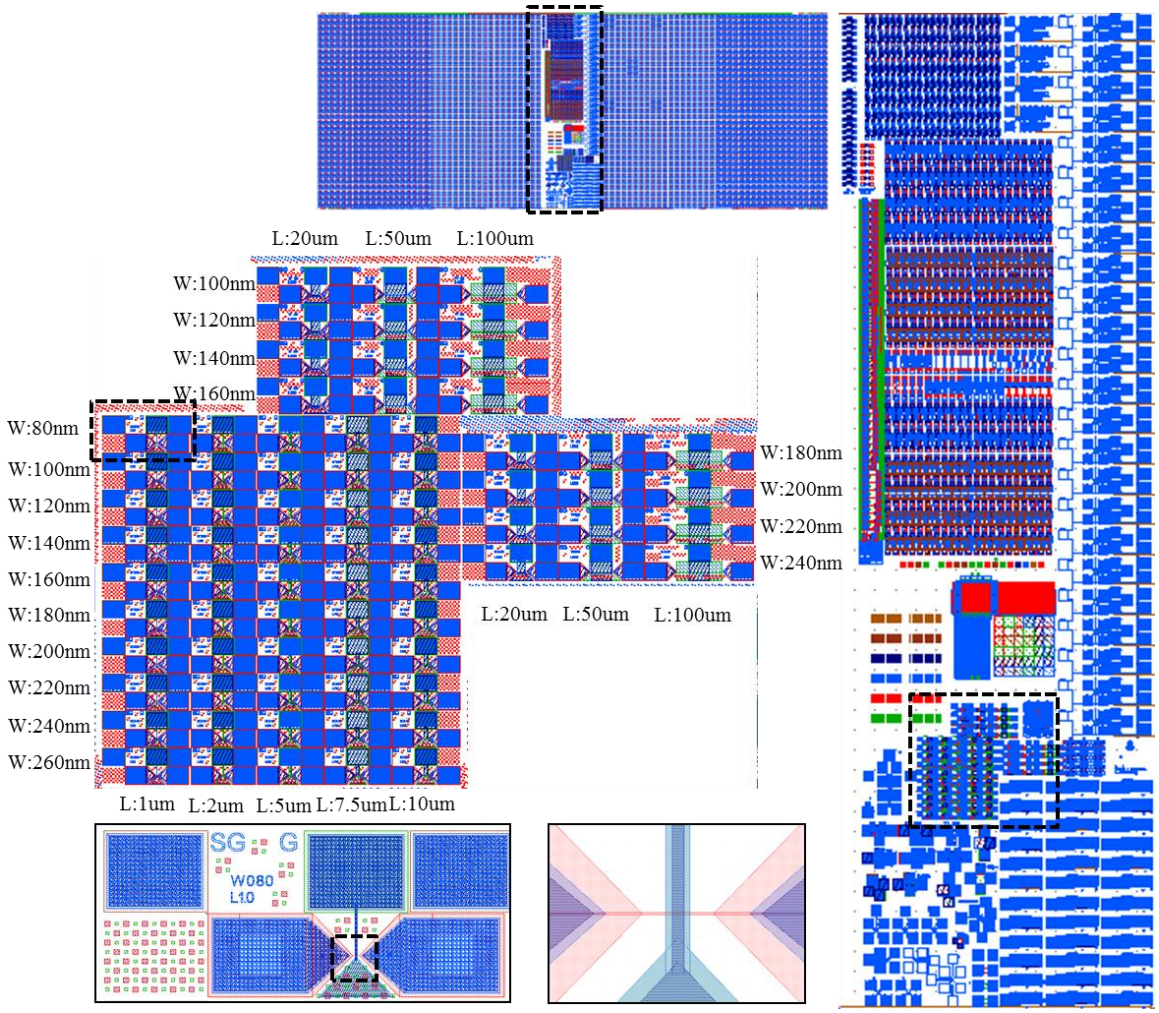


Figure 5.21. FET device arrays with big contacts.

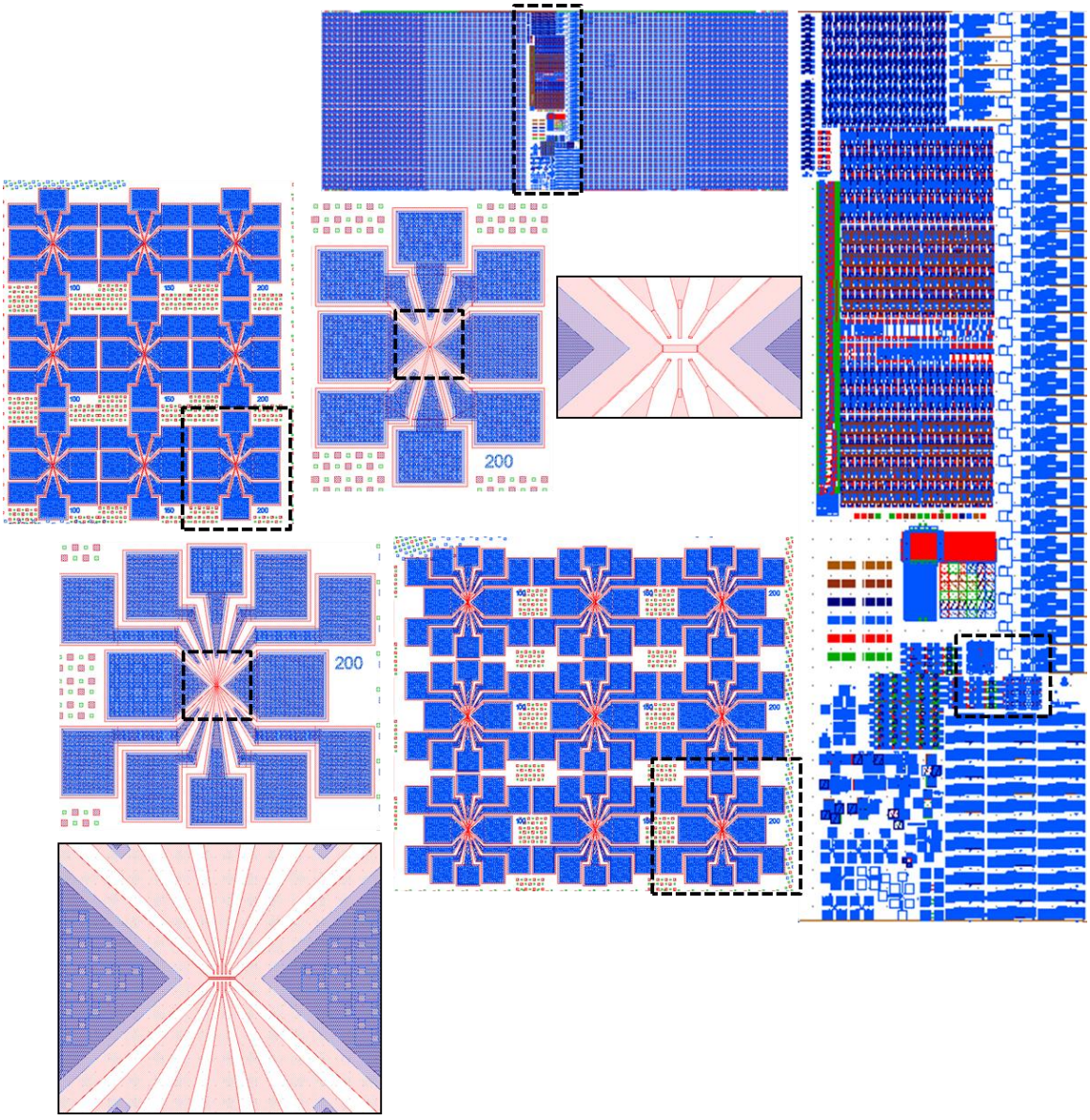


Figure 5.22. 8-12 contacts heater structures.

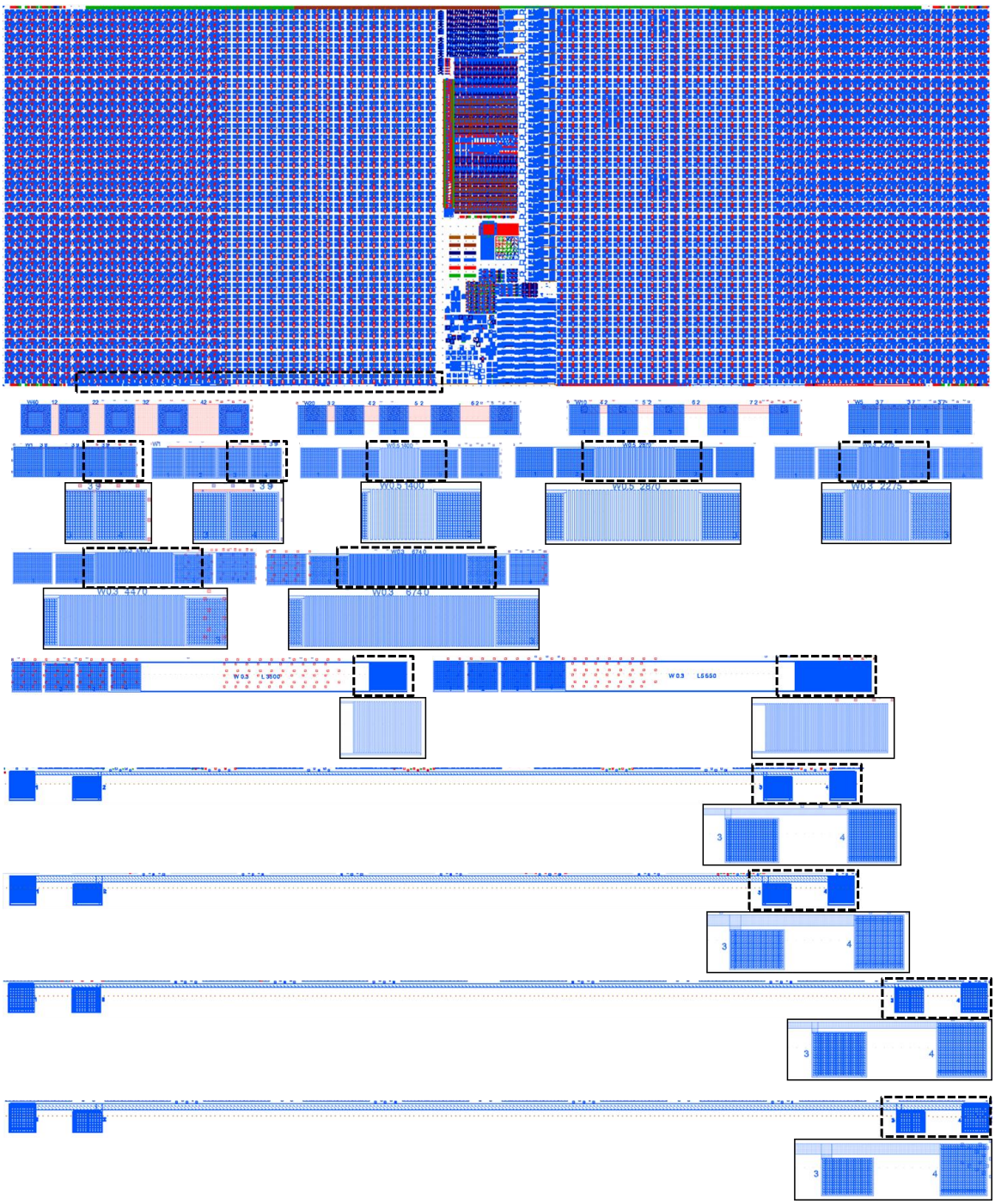


Figure 5.23. Big structures for film resistivity and metal resistivity measurements.

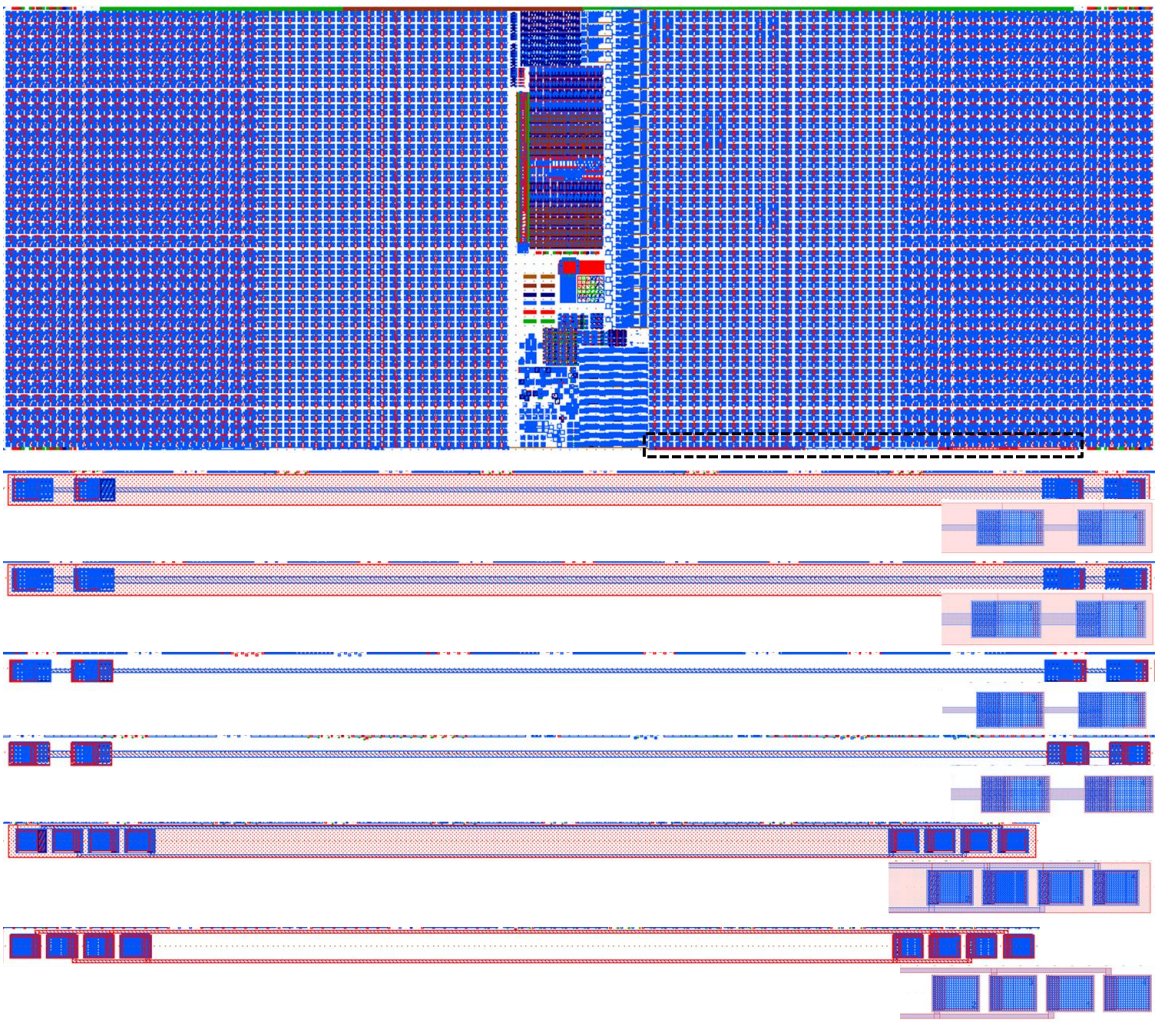


Figure 5.24. Thermal conductivity measurement structures.

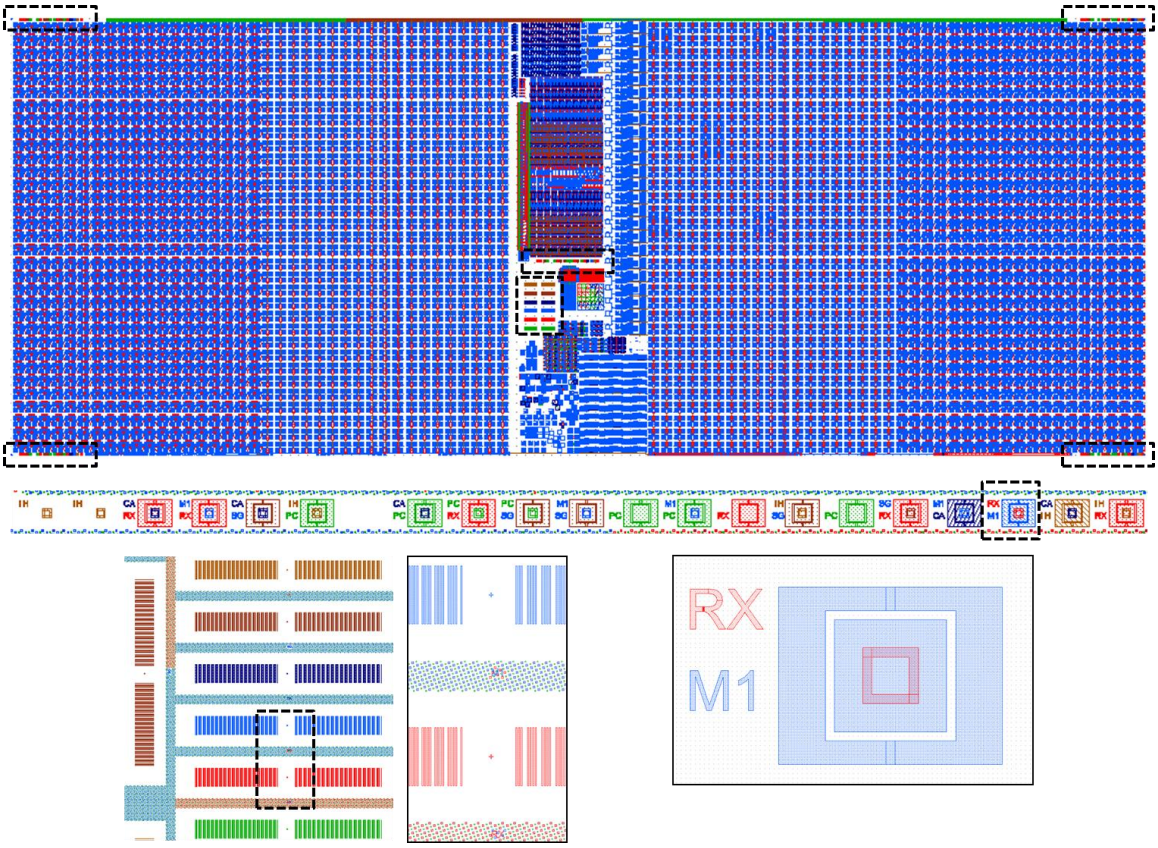


Figure 5.25. Vertical and horizontal alignment marks and overlay marks (corners and center)

5.2 Details of the mask design

Critical dimension is 60 nm for 5GATERXPCSG and 300 nm for 5GNEWCAM1IH reticles.

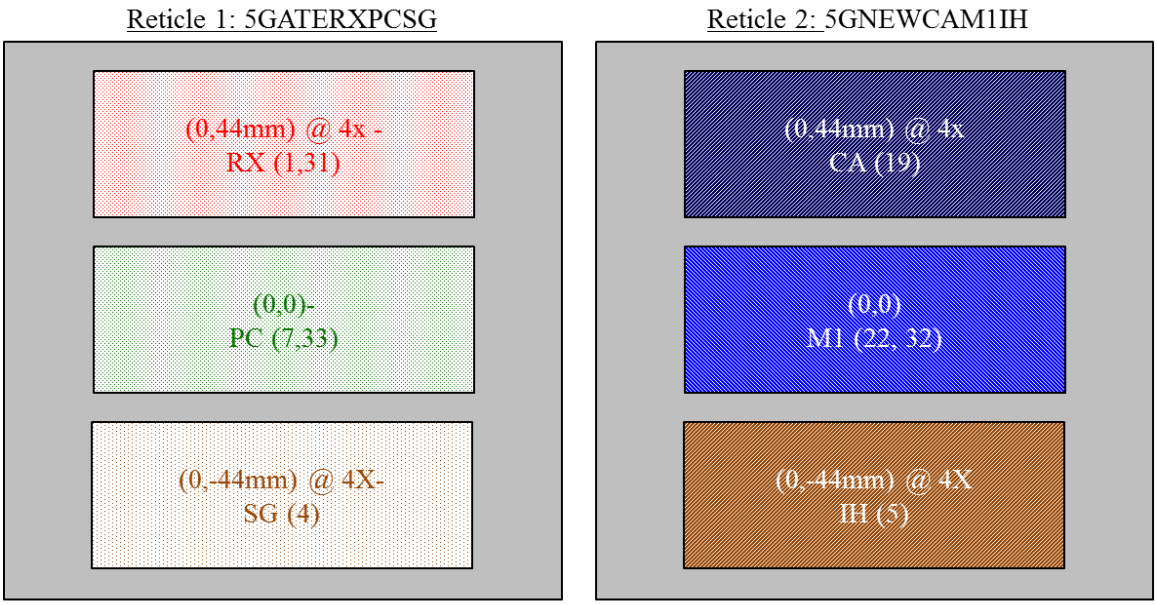


Figure 5.26. Schematics of printed reticles.

Table 5.5. Level information in redesigned reticles

Level name	Level number	Purpose	Reticle type
RX	1	Active area	Light field
RXFILL	31	Fillers (in the RX mask)	Light field
PC	7	Gate	Light field
PCFILL	33	Fillers (in the PC mask)	Light field
SG	4	Side gate	Light field
CA	19	Via	Dark field
M1	22	Metal	Dark field
M1FILL	32	Dark field	Dark field
IH	5	Side gate poly plug	Dark field

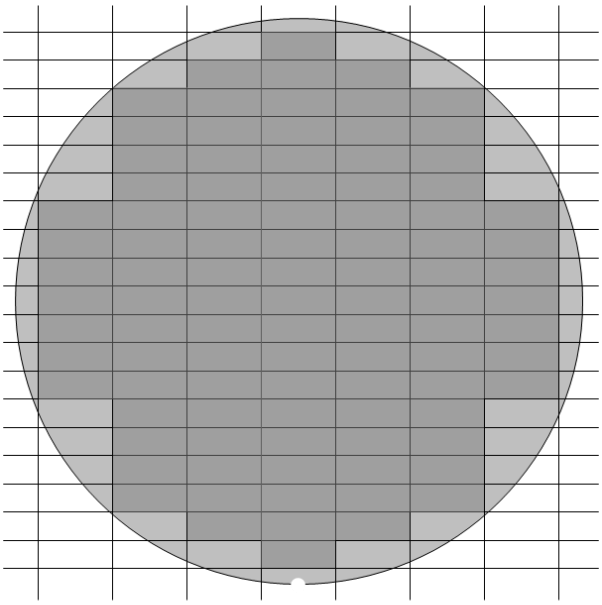


Figure 5.27. Schematic of the die arrangement on a 8 inches wafer (97 full Dies)

5.3 Details of the fabrication process

The details of the phase change memory device fabrication process are given in a table format as below.

Table 5.6. Detailed fabrication process

	Task	Process 1	Process 2	Process 3	Process 4
1	Clean	Ozone clean	Spin, rinse, dry		
2	Oxide deposition (test wafer)	600 nm Hot oxide			
3	Inspection	Ellipsometer	600 nm		
4	Oxide deposition (product wafers)	600 nm Hot oxide			
5	Inspection	Ellipsometer	600 nm		
6	Clean	Ozone clean	Spin, rinse, dry		
7	Lithography of M1 level (test wafer)	Coat resist	Expose (13 mJ, 0 µm)		

	Task	Process 1	Process 2	Process 3	Process 4
8	Inspection	SEM (JEOL)			
9	Lithography of M1 level (product wafers)	Coat resist	Expose (13 mJ, 0 μm)		
10	Inspection	SEM (JEOL)			
11	RIE (test wafer)	250 nm SiO_2 etch			
12	Inspection	Profilometer	SEM (JEOL)		
13	Strip resist	O_2 plasma			
14	Clean	Sulfiric Nitric clean	Ozone clean	Spin, rinse, dry	
15	Inspection	Profilometer	SEM (JEOL)		
16	RIE (product wafers)	250 nm SiO_2 etch			
17	Inspection	Profilometer	SEM (JEOL)		
18	Strip resist	O_2 plasma			
19	Clean	Sulfiric Nitric clean	Ozone clean	Spin, rinse, dry	
20	Inspection	Profilometer	SEM (JEOL)		
21	Metal deposition (test wafer)	10 nm TiN liner	600 nm W		
22	Metal deposition (test wafer)	150 nm CVD TiN	150 nm PVD TiN		
23	Inspection	SEM (ZEISS)			
24	Metal deposition (product wafers)	10 nm TiN liner	600 nm W		
25	Metal deposition (product wafers)	150 nm CVD TiN	150 nm PVD TiN		
26	Polish W (test wafer)	600 nm W CMP	10 nm TiN liner CMP		
27	Inspection	Optical microscope	Profilometer	Ellipsometer	SEM (JEOL)
28	Polish W (product wafers)	600 nm W CMP	10 nm TiN liner CMP		

	Task	Process 1	Process 2	Process 3	Process 4
29	Inspection	Optical microscope	Profilometer	Ellipsometer	SEM (ZEISS)
30	Polish TiN (test wafer)	300 nm TiN CMP			
31	Inspection	Optical microscope	Profilometer	Ellipsometer	SEM (JEOL)
32	Clean	Spin, rinse, dry			
33	Polish TiN (product wafers)	300 nm TiN CMP			
34	Inspection	Optical microscope	Profilometer	Ellipsometer	SEM (ZEISS)
35	Clean	Spin, rinse, dry			
36	GST deposition (product wafers)	GST (20, 50, 100 nm)	10 nm SiO_2 caping		
37	Clean	Spin, rinse, dry			
38	Si_3N_4 deposition (test wafers)	Si_3N_4 (20, 50, 100 nm)			
39	Inspection	Ellipsometer			
40	Si_3N_4 deposition (product wafers)	Si_3N_4 (20, 50, 100 nm)			
41	Clean	Spin, rinse, dry			
42	Lithography of RX level (test wafer)	Coat resist	Expose (10.15 mJ, -0.2 µm)		
43	Inspection	Overlay measure	SEM (JEOL)		
44	Lithography of RX level (product wafers)	Coat resist	Expose (10.15 mJ, -0.2 µm)		
45	Inspection	Overlay measure	SEM (JEOL)		
46	RIE (test wafers)	Si_3N_4 (20, 50, 100 nm) etch	SiO_2 (10 nm) etch	GST (20, 50, 100 nm) etch	Strip resist
47	Inspection	Profilometer	Ellipsometer	SEM (JEOL)	
48	RIE (product wafers)	Si_3N_4 (20, 50, 100 nm) etch	SiO_2 (10 nm) etch	GST (20, 50, 100 nm) etch	Strip resist
49	Inspection	Profilometer	Ellipsometer	SEM (JEOL)	

	Task	Process 1	Process 2	Process 3	Process 4
50	SiO_2 etch (some product wafers)	10:1 DHF (etch times vary)			
51	SiO_2 deposition (product wafers)	10 nm SiO_2 capping			
52	Inspection	SEM (JEOL, ZEISS)			

The detailed list of the fabricated devices is provided below:

PCMUCONK46 lot

First generation mask set is used for this lot. 600 nm thermally grown SiO_2 is used as substrate. Figure 5.28 shows the schematic illustration of the device's top view and cross section. Table 5.7 shows the list of the wafers/films used for this lot.

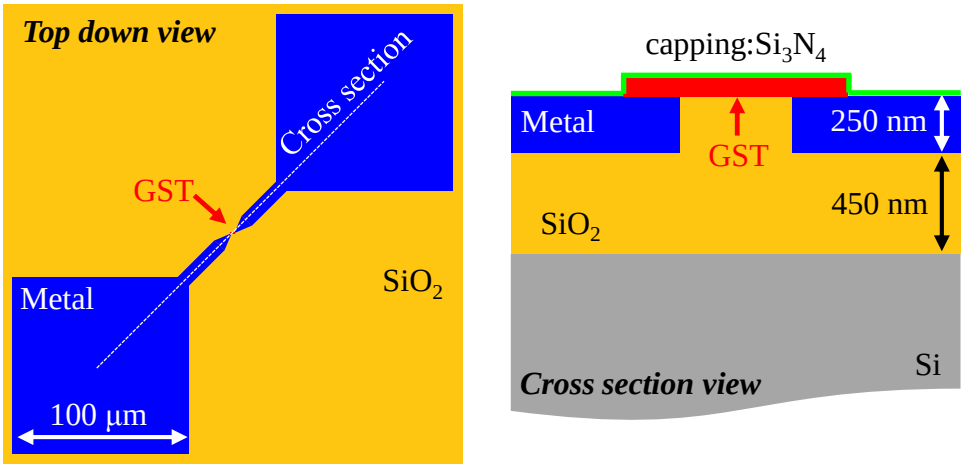


Figure 5.28. Schematic illustrations of the layout of the PCMUCONK46 lot.

Table 5.7. List of the wafers/films used for PCMUCONK46 lot.

Wafer #	Metal	GST thickness (nm)	capping	Additional info
1	CVD W/(Ti/TiN) liner	50	Si_3N_4	capped
2	CVD W/(Ti/TiN) liner	20	Si_3N_4	capped
3	CVD W/(Ti/TiN) liner	20	Si_3N_4	no cap, no DHF
4	CVD W/(Ti/TiN) liner	20	Si_3N_4	capped
5	CVD TiN+PVD TiN	20	Si_3N_4	5-1-1: capped
				5-1-2: DHF ~100nm
				5-1-3: DHF ~100nm
				5-2-1: no cap,no DHF
				5-3: DHF ~100nm
				5-4-1: capped
				5-4-2: DHF ~100nm
				5-4-3: DHF ~100nm
6	CVD TiN+PVD TiN	50	Si_3N_4	6-2: capped
				6-3: DHF ~100nm
				6-4-1: DHF ~100nm
				6-4-2: capped
7	scrapped (used for cross sectioning in earlier stage of fabrication)			
8	PVD TiN	50	Si_3N_4	large voids in metal
9	CVD W/(Ti/TiN) liner	50	Si_3N_4	9-1: no cap, no DHF
				9-2: capped
				9-3: DHF ~100nm
				9-4: capped

PCMUCONOXL22 lot

Second generation mask set is used for this lot. 600 nm thermally grown SiO_2 is used as substrate. Figure 5.29 shows the schematic illustration of the device's top view and cross section. Table 5.8 shows the list of the wafers/films used for this lot.

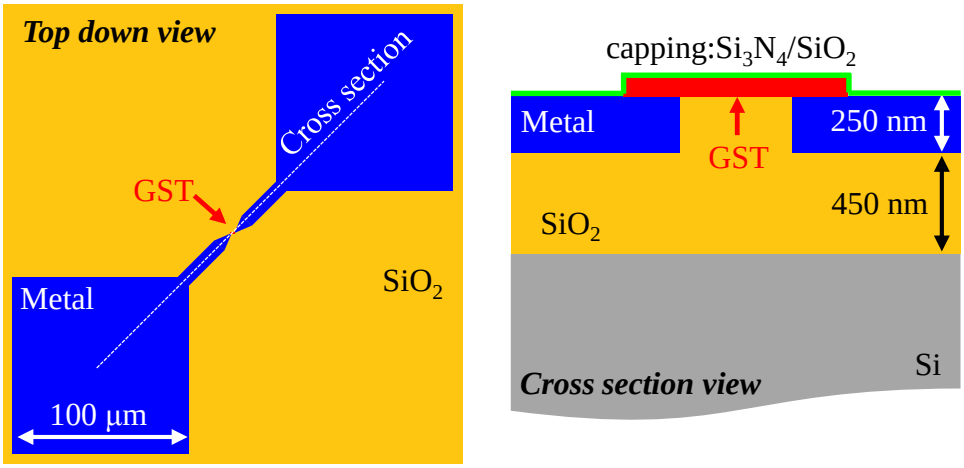


Figure 5.29. Schematic illustrations of the layout of the PCMUCONOXL22 lot.

Table 5.8. List of the wafers/films used for PCMUCONOXL22 lot.

Wafer #	Metal	GST thickness (nm)	capping	Additional info
1	CVD W/TiN liner	20	SiO_2	capped
2	CVD TiN+PVD TiN	20	SiO_2	
3	CVD W/TiN liner	50	SiO_2	3-2: capped
4	CVD TiN+PVD TiN	50	SiO_2	4-1: capped
5	CVD W/TiN liner	100	SiO_2	5-3: capped
6	scrapped (during GST etch)			
7	CVD W/TiN liner	20	SiO_2	7-2: capped
8	CVD TiN+PVD TiN	50	SiO_2	
9	CVD TiN+PVD TiN	100	SiO_2	

PCMUCONI2L41 lot (fabrication is being processed by Adam Cywar)

Second generation mask set used for this lot. 100 nm LPCVD low stress Si_3N_4 deposited on 600 nm thermally grown SiO_2 is and used as substrate. Figure 5.30 shows the schematic illustration of the device's top view and cross section. Table 5.9 shows the list of the wafers/films used for this lot.

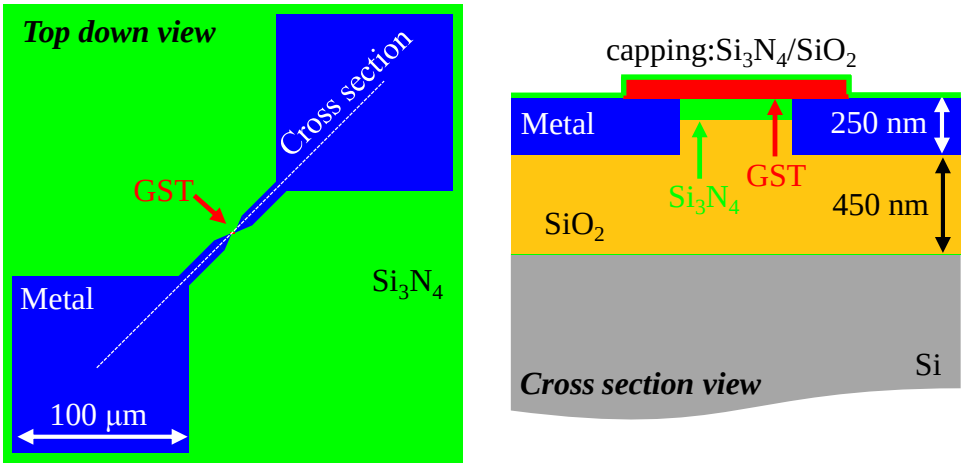


Figure 5.30. Schematic illustrations of the layout of the PCMUCONI2L41 lot.

Table 5.9. List of the wafers/films used for PCMUCONI2L41 lot.

Wafer #	Metal	GST thickness (nm)	capping	Additional info
1	CVD W/TiN liner	20	Si_3N_4	
2	CVD TiN+PVD TiN	20	Si_3N_4	
3	CVD W/TiN liner	50	Si_3N_4	
4	CVD TiN+PVD TiN	50	Si_3N_4	
5	CVD W/TiN liner	100	Si_3N_4	
6	CVD TiN+PVD TiN	100	Si_3N_4	
7	CVD W/TiN liner	20	Si_3N_4	
8	CVD TiN+PVD TiN	50	Si_3N_4	
9	CVD TiN+PVD TiN	100	Si_3N_4	

PCMUCONRT lots (these lots are designed for film measurements)

The largest opening square (2.048 mm x 2.048 mm) in IBM 248 nm Mixfiducial mask is used to open trenches for bottom electrodes (W). The same mask is used to etch metal level using image reversal lithography technique following metal deposition. Figure 5.31 shows the schematic illustration of the device's top view and cross section. Table 5.10 shows the list of the wafers/films used for this lot.

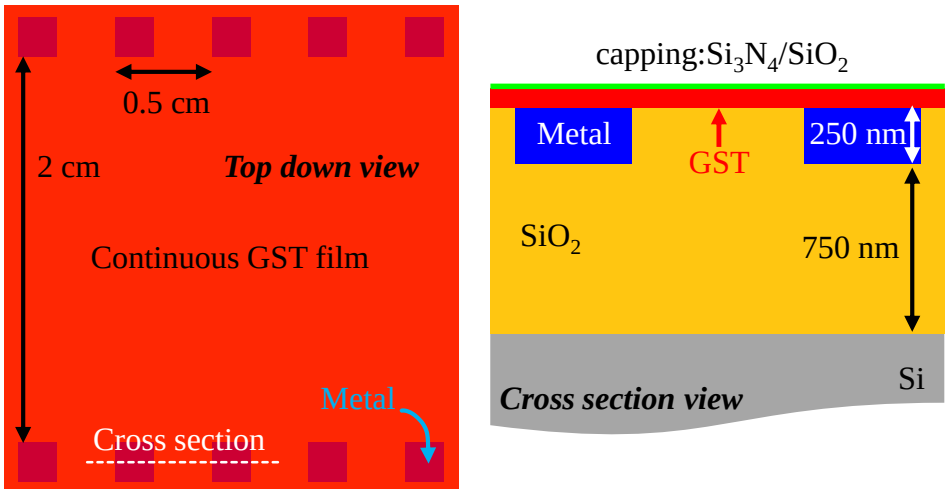


Figure 5.31. Schematic illustrations of the layout of the PCMUCONRT lots.

Table 5.10. List of the wafers/films used for PCMUCONRT lots.

Wafer #	Metal	GST thickness (nm)	capping	Additional info
Test_1	CVD W/(Ti/TiN) liner	100	SiO_2	50nm cap
Test_3	CVD W/(Ti/TiN) liner	50	SiO_2	25 nm cap
Test_4	CVD W/(Ti/TiN) liner	200	SiO_2	25 nm cap
M32_1	CVD W/(Ti/TiN) liner	15	Si_3N_4	10 nm cap
M32_2	CVD W/(Ti/TiN) liner	30	Si_3N_4	10 nm cap
M32_3	CVD W/(Ti/TiN) liner	50	Si_3N_4	10 nm cap
M32_4	CVD W/(Ti/TiN) liner	100	Si_3N_4	10 nm cap
M32_5	CVD W/(Ti/TiN) liner	15	Si_3N_4	10 nm cap
M32_6	CVD W/(Ti/TiN) liner	200	Si_3N_4	10 nm cap
M32_7	CVD W/(Ti/TiN) liner	200	Si_3N_4	10 nm cap
M32_8	CVD W/(Ti/TiN) liner	50	Si_3N_4	10 nm cap

5.4 Software tools developed using Labview for instrument control for electrical characterization

5.4.1 Function generator unit control program

A computer controlled Tektronix AFG 3102 Dual Channel Arbitrary/Function Generator is used in electrical characterization. Control programs used here has three

versions Front panels of each control programs are provided in Figure 5.32. Information such as file names, measurement parameters and user comments are saved in an index file. Oscilloscope parameters can be set using the same interface. Before applying the signal, waveform has to be loaded to the function generator by activating “reset parameters” button.

In the first version, preferred waveform is imported from a text file which can be generated using Originlab, and then interpolated on 131072 points (max length of the waveform is 128 K). Amplitudes of the waveform can be scaled using scaling control.

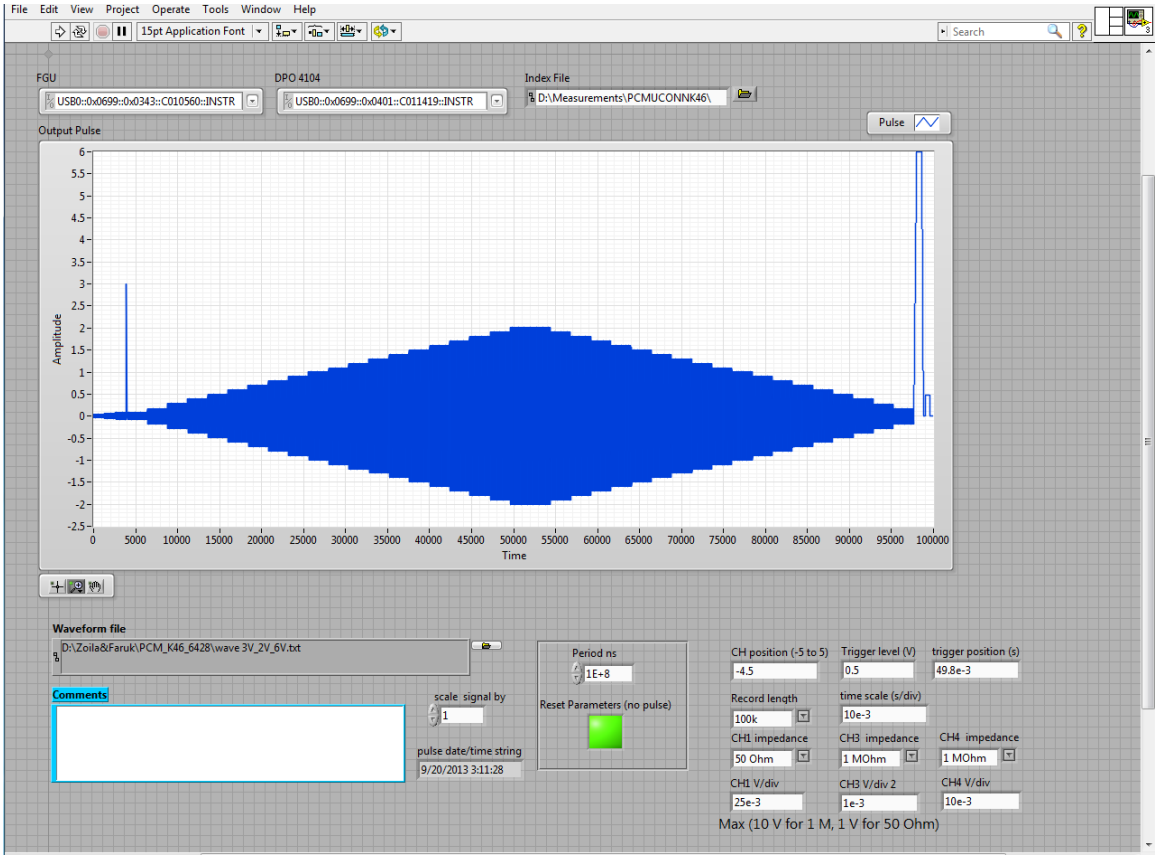


Figure 5.32. Front panel of FGU controller tool (arbitrary wave form).

In the second version, AC pre-pulse+pulse+AC post-pulse sequence of signals can be generated with the specified parameters. Hysteresis button provides AC segments after the pulse with the amplitudes are stepped up and then down.

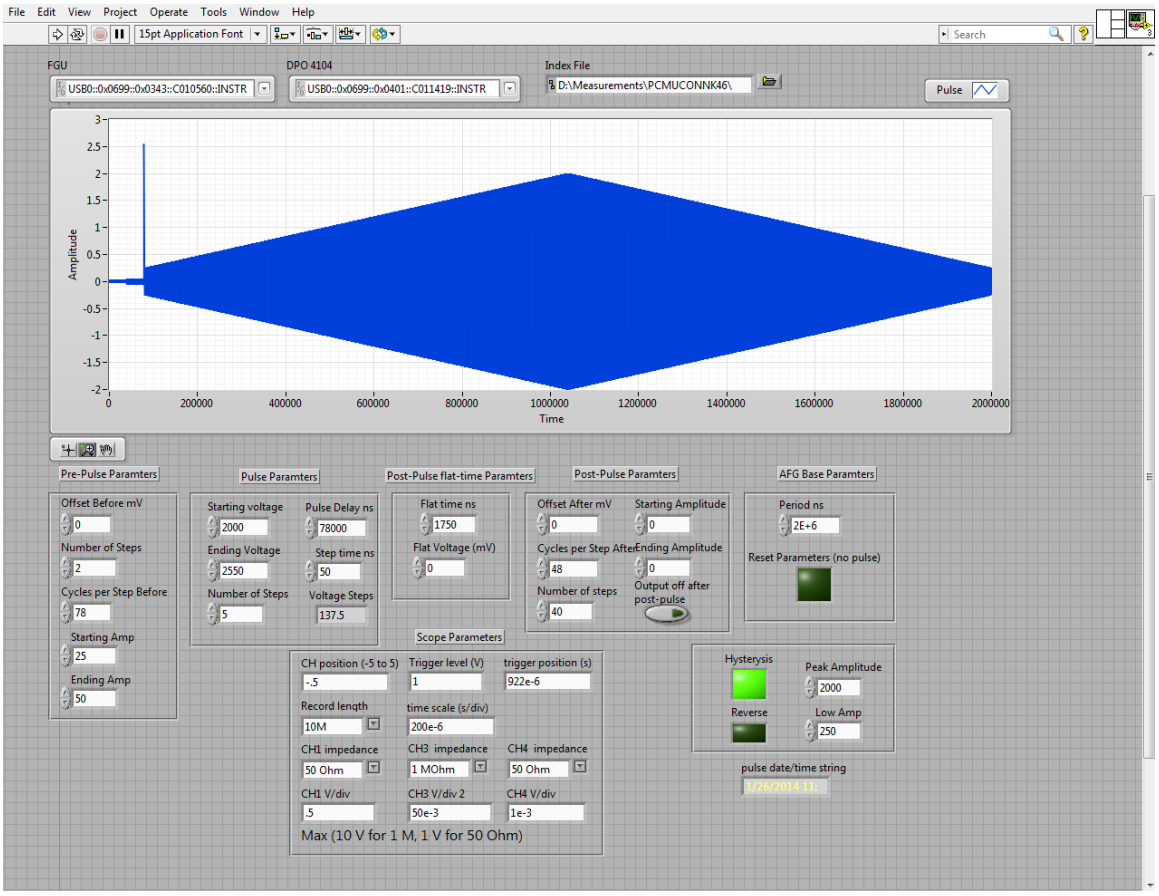


Figure 5.33. Front panel of FGU controller tool (AC pre-pulse+pulse+AC post-pulse).

In the third version, DC pre-pulse+pulse+DC post-pulse sequence of signals can be generated with the specified parameters. Hysteresis button provides DC segments after the pulse with the amplitudes are stepped up and then down.

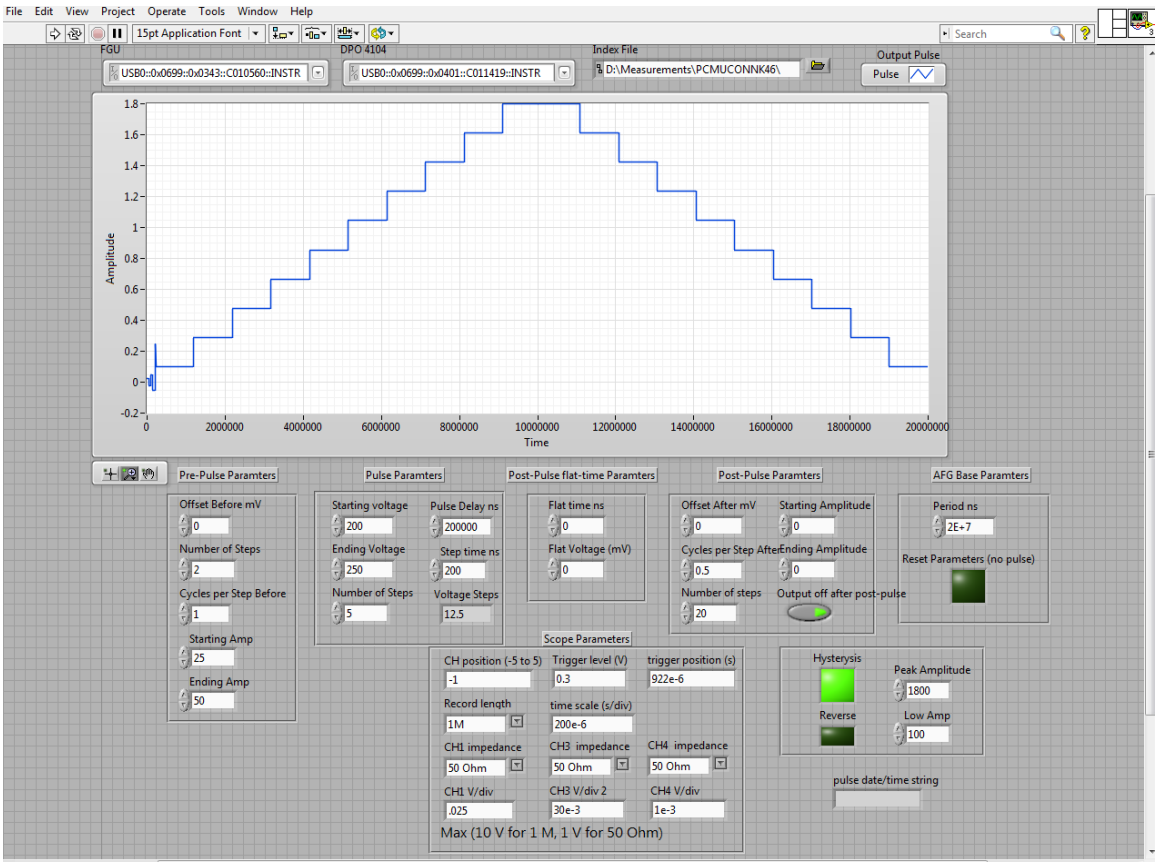


Figure 5.34. Front panel of FGU controller tool (DC pre-pulse+pulse+DC post-pulse).

5.4.2 Oscilloscope data acquisition program

A computer controlled Tektronix DPO410 oscilloscope is used in electrical characterization. . Front panel of control program is provided in Figure 5.35. Information such as file names and input values are saved in an index file. Measurements are saved with prefix in file path which is the directory name. Counter can be turned on or off for incremental data file names. Preferred channels can be selected by turning on and off "active" buttons. Average offsets can be extracted before the measurement by acquiring constant DC signals and then subtracted so the data can be calibrated. If the data length

10 million data points, “Acquire 10 M data?” led turns on and data is acquired as 10 equal segments sequent due to the large file size.

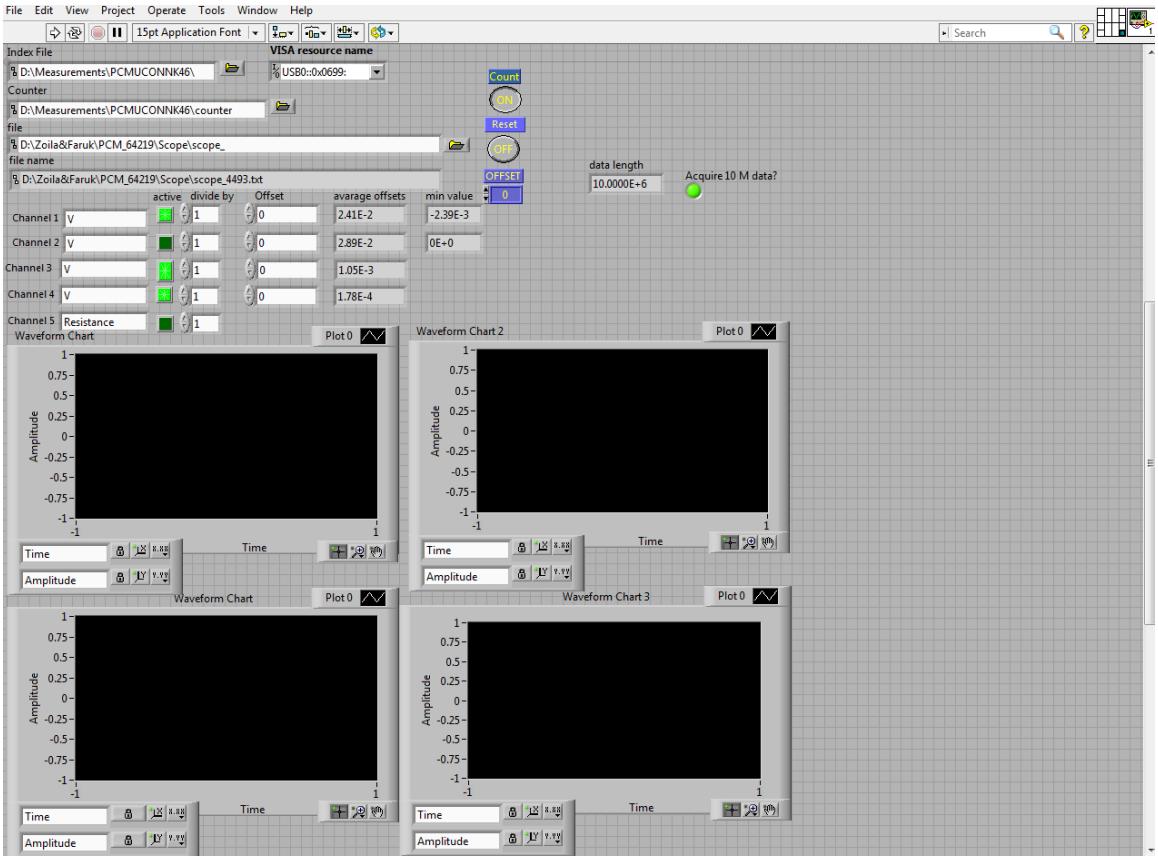


Figure 5.35. Front panel of Oscilloscope data acquisition tool.

5.4.3 DAQ card control program

A computer controlled National instruments 9219 DAQ card is used in electrical characterization. Front panel of control program is provided in Figure 5.36. Information such as file names and measurement parameters are saved in an index file. Measurements are saved with prefix in file path which is the directory name. Counter can be turned on or off for incremental data file names. Minimum voltage range can be adjusted between -100 mV and 100 mV. Maximum sampling rate is 100 S/s. Due to offset voltages vary for

each measurements, it has to be calibrated before each measurements Data read from channelX is plotted in chartsXA which is zoomed in view of chartXB.

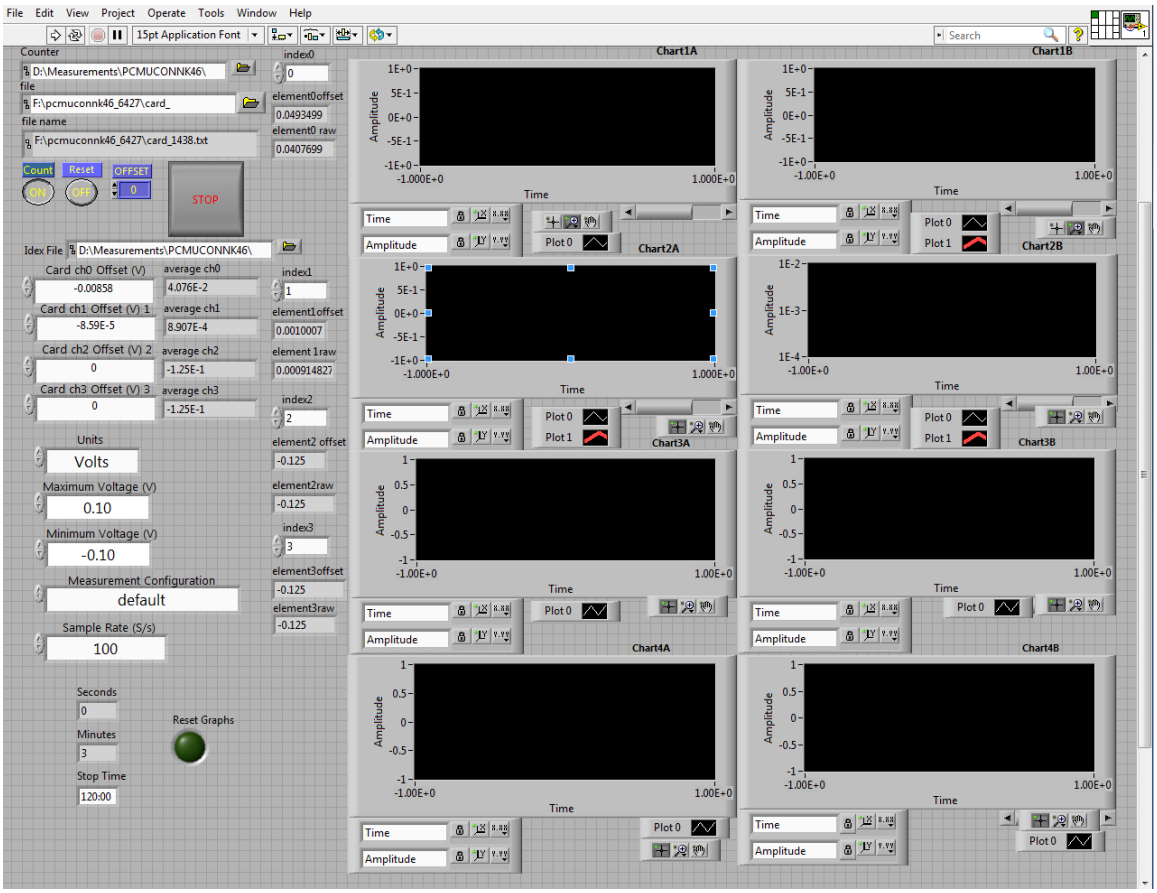


Figure 5.36. Front panel of DAQ card controller tool.

5.4.4 Parameter analyzer control program

A computer controlled HP 4145B and Agilent 4156C Parameter analyzers are used in electrical characterization. Front panel of control program is provided in Figure 5.37. The parameter analyzer program is modified version of Ali Gokirmak's parameter analyzer controller program developed for HP 4145B parameter analyzers. Information such as file names, measurement parameters, and user comments are saved in an index file. Measurements are saved with prefix in file path which is the directory name. Counter

can be turned on or off for incremental data file names. Parameter analyzer can be set to make single or multiple measurements by turning on and off the “single” button. Multiple measurements can be interrupted by “stop” button. SMUs and VMUs inputs must be set for required measurements.

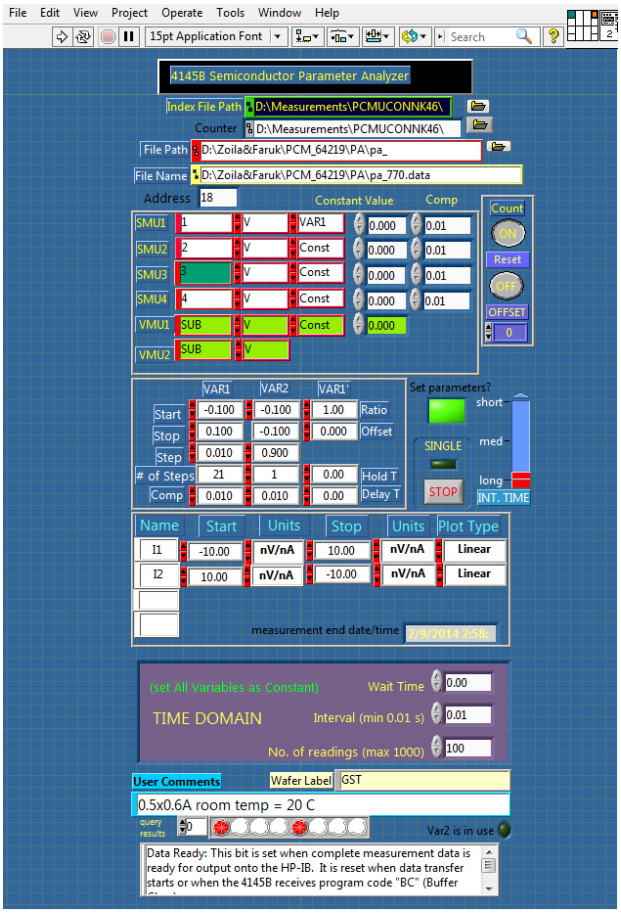


Figure 5.37. Front panel of HP4145B parameter analyzer controller tool.

5.4.5 Parameter analyzer data acquisition program

Parameter analysis data acquisition program is modified version of Ali Gokirmak’s MOSFET parameter extraction program however it is only used to extract device resistances from applied voltage sweeps through the devices by parameter analyzer. Front panel of control program is provided in Figure 5.38. Program can be

either called by the parameter analyzer control program or run independently. Information such as file names, input values and calculated parameters are saved in a parameter file. Multiple data sets can be plot on top of each other in a same graph by turning on and off “clear” button or using “counter” button specified starting and ending data number with suffix. Slope, intercept and calculated resistances values are located upper center of the window.

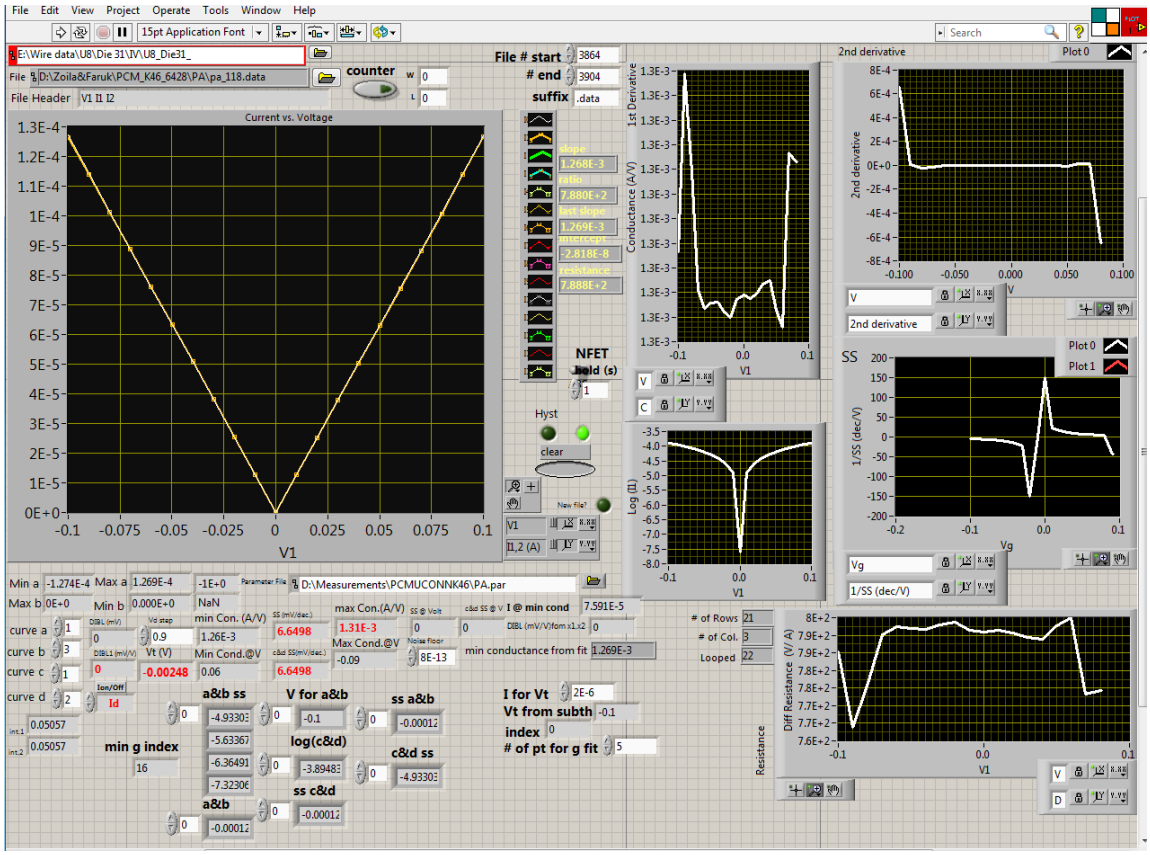


Figure 5.38. Front panel of parameter analyzer analysis tool.

5.5 Matlab codes

5.5.1 Main analysis code

%------------------(by Gokhan Bakan, Faruk Dirisaglik, Sadid Muneer)------------------%

close all

```
clc
clear
 %----------------------Loading Data in Memory-----------------------%
 dataFile         = input('Please enter data file: ', 's')
inputFile         = [dataFile '.txt']
DataLoadingStartTime = datestr(clock);
[time Ch1r V2 Ch2r V4 Ch3r V6 Ch4r V8 R] = textread(inputFile,...
    '%f %f %f %f %f %f %f %f %f %f','headerlines',1,'delimiter','\t');
DataLoadingEndTime = datestr(clock);
clear('time','V2', 'V4', 'V6', 'V8', 'R' )
% Zero triggering is at 79.998us (@ 399,991 datapoint)
f         = 1e6;          % applied sinusoidal frequency
Sc        = 5000;         % samples per cycle
cycles    = 48;           % cySces per step
Sst       = Sc*cycles;    % samples per step
Ch1sft    = -5 ;          % Shift of Ch1 from pulse start (point 400,001)
Ch2sft    = 30 ;          % Shift of Ch2 from pulse start (point 400,001)
Ch3sft    = 20 ;          % Shift of Ch3 from pulse start (point 400,001)
Ch4sft    = -5 ;          % Shift of Ch4 from pulse start (point 400,001)
C_ter     = 214e-12;      % Total Capacitance of the termination elements (in F)
D_C_ter   = 23e-12;       % Error in total capacitance of the termination elements (in F)
R_ter     = 51.9;         % Total resistance of the termination elements (in Ohms)
D_R_ter   = 1;            % Error in total resistance of the termination elements (in Ohms)
R_load    = 1000;         % Load resistor (in Ohms)
D_R_load  = 5;            % Uncertainity in load resistor (in Ohms)
C_load    = 750e-15;      % Load capacitance (in F)
D_C_load  = 20e-15;       % Uncertainity in load capacitance (in F)
Z_int_broken_r      = -5.6e5;       % real part of Z_int from broken wires
D_Z_int_broken_r    = 50e3;         % Uncertainity real part of Z_int from broken wires
Z_int_broken_i      = -4.8e6;       % imaginary part of Z_int from broken wires
D_Z_int_broken_i    = 100e3;        % imaginary part of Z_int from broken wires
```

```
R_sub  = Z_int_broken_r;                % Substrate resistance (in Ohms)
D_R_sub= D_Z_int_broken_r;              % Uncertainity in substrate resistance (in Ohms)
C_sub= -1/(2*pi*f*Z_int_broken_i); % Pad capacitance (in F)
D_C_sub= D_Z_int_broken_i/(2*pi*f*Z_int_broken_i^2);  % Uncertainity in pad
capacitance (in F)

%--------------Getting data from correct starting points--------------%
 % This block fixes after pulse voltage starting points for Ch1-Ch4
Vst_Ch1 = 400001 + Ch1sft;
Vst_Ch2 = 400001 + Ch2sft;
Vst_Ch3 = 400001 + Ch3sft;
Vst_Ch4 = 400001 + Ch4sft;

% This block extracts 1919 cycles from after pulse voltage starting point for Ch1-Ch4

Ch1 = Ch1r(Vst_Ch1:Vst_Ch1+1919*5000);
Ch2 = Ch2r(Vst_Ch2:Vst_Ch2+1919*5000);
Ch3 = Ch3r(Vst_Ch3:Vst_Ch3+1919*5000);
Ch4 = Ch4r(Vst_Ch4:Vst_Ch4+1919*5000);

%-------------------------Voltage Fits-------------------------------%
%sine fitting with 0 and 90 degress phases
[V1_0deg D_V1_0deg V1_offset_0deg D_V1_offset_0deg V1_RMSE_0deg] =
sine_fit_alt(Ch1, 0);
[V1_90deg D_V1_90deg V1_offset_90deg D_V1_offset_90deg V1_RMSE_90deg] =
sine_fit_alt(Ch1, pi/2);

[V2_0deg D_V2_0deg V2_offset_0deg D_V2_offset_0deg V2_RMSE_0deg] =
sine_fit_alt(Ch2, 0);
[V2_90deg D_V2_90deg V2_offset_90deg D_V2_offset_90deg V2_RMSE_90deg] =
sine_fit_alt(Ch2, pi/2);
```

```
[V3_0deg D_V3_0deg V3_offset_0deg D_V3_offset_0deg V3_RMSE_0deg] =
sine_fit_alt(Ch3, 0);
[V3_90deg D_V3_90deg V3_offset_90deg D_V3_offset_90deg V3_RMSE_90deg] =
sine_fit_alt(Ch3, pi/2);

[V4_0deg D_V4_0deg V4_offset_0deg D_V4_offset_0deg V4_RMSE_0deg] =
sine_fit_alt(Ch4, 0);
[V4_90deg D_V4_90deg V4_offset_90deg D_V4_offset_90deg V4_RMSE_90deg] =
sine_fit_alt(Ch4, pi/2);

% extraction of actual phase in the signals. 0 and 90 degrees of sine
% phases are converted to -90 and 0 degrees of cosine phases to work with
% complex numbers. then pi/2 is added to come back to sine phase

V1_phase = angle(V1_0deg*exp(1i*(0-pi/2))+V1_90deg*exp(1i*(pi/2-pi/2))) + pi/2;
V2_phase = angle(V2_0deg*exp(1i*(0-pi/2))+V2_90deg*exp(1i*(pi/2-pi/2))) + pi/2;
V3_phase = angle(V3_0deg*exp(1i*(0-pi/2))+V3_90deg*exp(1i*(pi/2-pi/2))) + pi/2;
V4_phase = angle(V4_0deg*exp(1i*(0-pi/2))+V4_90deg*exp(1i*(pi/2-pi/2))) + pi/2;

%sine fitting with actual phases (from the largest voltage step)

V1_fit_phase =  mean(V1_phase(19:20));
V2_fit_phase =  mean(V2_phase(19:20));
V3_fit_phase =  mean(V3_phase(19:20));
V4_fit_phase =  mean(V4_phase(19:20));
[V1 D_V1 V1_offset D_V1_offset V1_RMSE] = sine_fit_alt(Ch1,V1_fit_phase);
[V2 D_V2 V2_offset D_V2_offset V2_RMSE] = sine_fit_alt(Ch2,V2_fit_phase);
[V3 D_V3 V3_offset D_V3_offset V3_RMSE] = sine_fit_alt(Ch3,V3_fit_phase);
[V4 D_V4 V4_offset D_V4_offset V4_RMSE] = sine_fit_alt(Ch4,V4_fit_phase);
```

```
% Real and imaginary parts of V4 and error in V4. Here we are changing our reference from cosine to sine and subtracting V1 phase from V4 phase since we assume V1 is purely real.

V2_r = real(V2*exp(1i*(V2_fit_phase - V1_fit_phase)));
V2_i = imag(V2*exp(1i*(V2_fit_phase - V1_fit_phase)));
D_V2_r = real(D_V2*exp(1i*(V2_fit_phase - V1_fit_phase)));
D_V2_i = imag(D_V2*exp(1i*(V2_fit_phase - V1_fit_phase)));

V3_r = real(V3*exp(1i*(V3_fit_phase - V1_fit_phase)));
V3_i = imag(V3*exp(1i*(V3_fit_phase - V1_fit_phase)));
D_V3_r = real(D_V3*exp(1i*(V3_fit_phase - V1_fit_phase)));
D_V3_i = imag(D_V3*exp(1i*(V3_fit_phase - V1_fit_phase)));

V4_r = real(V4*exp(1i*(V4_fit_phase - V1_fit_phase)));
V4_i = imag(V4*exp(1i*(V4_fit_phase - V1_fit_phase)));
D_V4_r = real(D_V4*exp(1i*(V4_fit_phase - V1_fit_phase)));
D_V4_i = imag(D_V4*exp(1i*(V4_fit_phase - V1_fit_phase)));

% Calculation of real and imaginary components of current with error

[I2_r D_I2_r I2_i D_I2_i] = find_I10 (V2_r, D_V2_r, V2_i, D_V2_i, R_ter, D_R_ter, C_ter, D_C_ter, f);
IV2_matrix_r = [V1',D_V1',I2_r',D_I2_r'];
IV2_matrix_i = [V1',D_V1',I2_i',D_I2_i'];
figure
errorbar(V1,I2_r,D_I2_r)
hold on
errorbar(V1,I2_i,D_I2_i, 'r')
```

```
[I3_r D_I3_r I3_i D_I3_i] = find_I10 (V3_r, D_V3_r, V3_i, D_V3_i, R_ter, D_R_ter,
C_ter, D_C_ter, f);
IV3_matrix_r = [V1',D_V1',I3_r',D_I3_r'];
IV3_matrix_i = [V1',D_V1',I3_i',D_I3_i'];
figure
errorbar(V1,I3_r,D_I3_r)
hold on
errorbar(V1,I3_i,D_I3_i, 'r')

[I4_r D_I4_r I4_i D_I4_i] = find_I10 (V4_r, D_V4_r, V4_i, D_V4_i, R_ter, D_R_ter,
C_ter, D_C_ter, f);
IV4_matrix_r = [V1',D_V1',I4_r',D_I4_r'];
IV4_matrix_i = [V1',D_V1',I4_i',D_I4_i'];
figure
errorbar(V1,I4_r,D_I4_r)
hold on
errorbar(V1,I4_i,D_I4_i, 'r')

% Calculation of individual resistances for each step from complex current

omeg = 2*pi*f;
Ifaruk = I4_r + 1i*I4_i;
Ztotalfaruk = V1./Ifaruk;
Z_ter = (1/R_ter+1i*omeg*C_ter)^-1;
Z_loadfaruk = (1/R_load+1i*omeg*C_load)^-1;
Z_subfaruk = Z_int_broken_r + 1i*Z_int_broken_i;
Z_intfaruk = Ztotalfaruk-Z_ter-Z_loadfaruk;
Zwfaruk = Z_intfaruk*Z_subfaruk./(Z_subfaruk-Z_intfaruk);
Z_w_rfaruk = real(Zwfaruk);
Z_w_ifaruk = imag(Zwfaruk);
R_wfaruk = Z_w_rfaruk.*(1+Z_w_ifaruk.^2./Z_w_rfaruk.^2);
```

```
% Calculation of real and imaginary conductance using previously found
% current and error in current for all I points (40)

[IV2_40_r_offset, D_IV2_40_r_offset, Cond2_40_r, D_Cond2_40_r] =
york_fit10(V1,D_V1,I2_r,D_I2_r);
[IV2_40_i_offset, D_IV2_40_i_offset, Cond2_40_i, D_Cond2_40_i] =
york_fit10(V1,D_V1,I2_i,D_I2_i);

[IV3_40_r_offset, D_IV3_40_r_offset, Cond3_40_r, D_Cond3_40_r] =
york_fit10(V1,D_V1,I3_r,D_I3_r);
[IV3_40_i_offset, D_IV3_40_i_offset, Cond3_40_i, D_Cond3_40_i] =
york_fit10(V1,D_V1,I3_i,D_I3_i);

[IV4_40_r_offset, D_IV4_40_r_offset, Cond4_40_r, D_Cond4_40_r] =
york_fit10(V1,D_V1,I4_r,D_I4_r);
[IV4_40_i_offset, D_IV4_40_i_offset, Cond4_40_i, D_Cond4_40_i] =
york_fit10(V1,D_V1,I4_i,D_I4_i);

% Calculation of real and imaginary conductance using previously found
% current and error in current for (20) points

w_s20 = 20;              % linear fit of first 20 points

[IV2_f20_r_offset, D_IV2_f20_r_offset, Cond2_f20_r, D_Cond2_f20_r] =
york_fit10(V1(1:w_s20),D_V1(1:w_s20),I2_r(1:w_s20),D_I2_r(1:w_s20));
[IV2_f20_i_offset, D_IV2_f20_i_offset, Cond2_f20_i, D_Cond2_f20_i] =
york_fit10(V1(1:w_s20),D_V1(1:w_s20),I2_i(1:w_s20),D_I2_i(1:w_s20));

[IV3_f20_r_offset, D_IV3_f20_r_offset, Cond3_f20_r, D_Cond3_f20_r] =
york_fit10(V1(1:w_s20),D_V1(1:w_s20),I3_r(1:w_s20),D_I3_r(1:w_s20));
```

```
[IV3_f20_i_offset, D_IV3_f20_i_offset, Cond3_f20_i, D_Cond3_f20_i] =
york_fit10(V1(1:w_s20),D_V1(1:w_s20),I3_i(1:w_s20),D_I3_i(1:w_s20));

[IV4_f20_r_offset, D_IV4_f20_r_offset, Cond4_f20_r, D_Cond4_f20_r] =
york_fit10(V1(1:w_s20),D_V1(1:w_s20),I4_r(1:w_s20),D_I4_r(1:w_s20));
[IV4_f20_i_offset, D_IV4_f20_i_offset, Cond4_f20_i, D_Cond4_f20_i] =
york_fit10(V1(1:w_s20),D_V1(1:w_s20),I4_i(1:w_s20),D_I4_i(1:w_s20));

a_l20 = numel (V1);    % linear fit of last 20 points

[IV2_l20_r_offset, D_IV2_l20_r_offset, Cond2_l20_r, D_Cond2_l20_r] =
york_fit10(V1(a_l20-w_s20+1:a_l20),D_V1(a_l20-w_s20+1:a_l20),I2_r(a_l20-
w_s20+1:a_l20),D_I2_r(a_l20-w_s20+1:a_l20));
[IV2_l20_i_offset, D_IV2_l20_i_offset, Cond2_l20_i, D_Cond2_l20_i] =
york_fit10(V1(a_l20-w_s20+1:a_l20),D_V1(a_l20-w_s20+1:a_l20),I2_i(a_l20-
w_s20+1:a_l20),D_I2_i(a_l20-w_s20+1:a_l20));

[IV3_l20_r_offset, D_IV3_l20_r_offset, Cond3_l20_r, D_Cond3_l20_r] =
york_fit10(V1(a_l20-w_s20+1:a_l20),D_V1(a_l20-w_s20+1:a_l20),I3_r(a_l20-
w_s20+1:a_l20),D_I3_r(a_l20-w_s20+1:a_l20));
[IV3_l20_i_offset, D_IV3_l20_i_offset, Cond3_l20_i, D_Cond3_l20_i] =
york_fit10(V1(a_l20-w_s20+1:a_l20),D_V1(a_l20-w_s20+1:a_l20),I3_i(a_l20-
w_s20+1:a_l20),D_I3_i(a_l20-w_s20+1:a_l20));

[IV4_l20_r_offset, D_IV4_l20_r_offset, Cond4_l20_r, D_Cond4_l20_r] =
york_fit10(V1(a_l20-w_s20+1:a_l20),D_V1(a_l20-w_s20+1:a_l20),I4_r(a_l20-
w_s20+1:a_l20),D_I4_r(a_l20-w_s20+1:a_l20));
[IV4_l20_i_offset, D_IV4_l20_i_offset, Cond4_l20_i, D_Cond4_l20_i] =
york_fit10(V1(a_l20-w_s20+1:a_l20),D_V1(a_l20-w_s20+1:a_l20),I4_i(a_l20-
w_s20+1:a_l20),D_I4_i(a_l20-w_s20+1:a_l20));
```

```
% Calculation of real and imaginary conductance using previously found
% current and error in current for (10) points

w_s10 = 10;              % linear fit of first 10 points

[IV2_f10_r_offset, D_IV2_f10_r_offset, Cond2_f10_r, D_Cond2_f10_r] =
york_fit10(V1(1:w_s10),D_V1(1:w_s10),I2_r(1:w_s10),D_I2_r(1:w_s10));
[IV2_f10_i_offset, D_IV2_f10_i_offset, Cond2_f10_i, D_Cond2_f10_i] =
york_fit10(V1(1:w_s10),D_V1(1:w_s10),I2_i(1:w_s10),D_I2_i(1:w_s10));

[IV3_f10_r_offset, D_IV3_f10_r_offset, Cond3_f10_r, D_Cond3_f10_r] =
york_fit10(V1(1:w_s10),D_V1(1:w_s10),I3_r(1:w_s10),D_I3_r(1:w_s10));
[IV3_f10_i_offset, D_IV3_f10_i_offset, Cond3_f10_i, D_Cond3_f10_i] =
york_fit10(V1(1:w_s10),D_V1(1:w_s10),I3_i(1:w_s10),D_I3_i(1:w_s10));

[IV4_f10_r_offset, D_IV4_f10_r_offset, Cond4_f10_r, D_Cond4_f10_r] =
york_fit10(V1(1:w_s10),D_V1(1:w_s10),I4_r(1:w_s10),D_I4_r(1:w_s10));
[IV4_f10_i_offset, D_IV4_f10_i_offset, Cond4_f10_i, D_Cond4_f10_i] =
york_fit10(V1(1:w_s10),D_V1(1:w_s10),I4_i(1:w_s10),D_I4_i(1:w_s10));

a_l10 = numel (V1);   % linear fit of last 10 points

[IV2_l10_r_offset, D_IV2_l10_r_offset, Cond2_l10_r, D_Cond2_l10_r] =
york_fit10(V1(a_l10-w_s10+1:a_l10),D_V1(a_l10-w_s10+1:a_l10),I2_r(a_l10-
w_s10+1:a_l10),D_I2_r(a_l10-w_s10+1:a_l10));
[IV2_l10_i_offset, D_IV2_l10_i_offset, Cond2_l10_i, D_Cond2_l10_i] =
york_fit10(V1(a_l10-w_s10+1:a_l10),D_V1(a_l10-w_s10+1:a_l10),I2_i(a_l10-
w_s10+1:a_l10),D_I2_i(a_l10-w_s10+1:a_l10));
```

```
[IV3_l10_r_offset, D_IV3_l10_r_offset, Cond3_l10_r, D_Cond3_l10_r] =
york_fit10(V1(a_l10-w_s10+1:a_l10),D_V1(a_l10-w_s10+1:a_l10),I3_r(a_l10-
w_s10+1:a_l10),D_I3_r(a_l10-w_s10+1:a_l10));
[IV3_l10_i_offset, D_IV3_l10_i_offset, Cond3_l10_i, D_Cond3_l10_i] =
york_fit10(V1(a_l10-w_s10+1:a_l10),D_V1(a_l10-w_s10+1:a_l10),I3_i(a_l10-
w_s10+1:a_l10),D_I3_i(a_l10-w_s10+1:a_l10));

[IV4_l10_r_offset, D_IV4_l10_r_offset, Cond4_l10_r, D_Cond4_l10_r] =
york_fit10(V1(a_l10-w_s10+1:a_l10),D_V1(a_l10-w_s10+1:a_l10),I4_r(a_l10-
w_s10+1:a_l10),D_I4_r(a_l10-w_s10+1:a_l10));
[IV4_l10_i_offset, D_IV4_l10_i_offset, Cond4_l10_i, D_Cond4_l10_i] =
york_fit10(V1(a_l10-w_s10+1:a_l10),D_V1(a_l10-w_s10+1:a_l10),I4_i(a_l10-
w_s10+1:a_l10),D_I4_i(a_l10-w_s10+1:a_l10));

% Error propagation into Zt, Zint, Zw, Rw and Cw

[Z_w_2_40, D_Z_w_2_40_r, D_Z_w_2_40_i, R_w_2_40, D_R_w_2_40, C_w_2_40,
D_C_w_2_40, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r, D_Z_ter_i,
Z_int_2_40, D_Z_int_2_40_r, D_Z_int_2_40_i] = Find_Zw_with_error10(f,
Cond2_40_r, D_Cond2_40_r, Cond2_40_i, D_Cond2_40_i, R_load, D_R_load, C_load,
D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub, D_R_sub, C_sub, D_C_sub);

[Z_w_2_f20, D_Z_w_2_f20_r, D_Z_w_2_f20_i, R_w_2_f20, D_R_w_2_f20,
C_w_2_f20, D_C_w_2_f20, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r,
D_Z_ter_i, Z_int_2_f20, D_Z_int_2_f20_r, D_Z_int_2_f20_i] =
Find_Zw_with_error10(f,Cond2_f20_r,D_Cond2_f20_r, Cond2_f20_i, D_Cond2_f20_i,
R_load, D_R_load, C_load, D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub,
D_R_sub, C_sub, D_C_sub);

[Z_w_2_l20, D_Z_w_2_l20_r, D_Z_w_2_l20_i, R_w_2_l20, D_R_w_2_l20,
C_w_2_l20, D_C_w_2_l20, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r,
```

D_Z_ter_i, Z_int_2_l20, D_Z_int_2_l20_r, D_Z_int_2_l20_i] =
Find_Zw_with_error10(f,Cond2_l20_r,D_Cond2_l20_r, Cond2_l20_i, D_Cond2_l20_i,
R_load, D_R_load, C_load, D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub,
D_R_sub, C_sub, D_C_sub);

[Z_w_2_f10, D_Z_w_2_f10_r, D_Z_w_2_f10_i, R_w_2_f10, D_R_w_2_f10,
C_w_2_f10, D_C_w_2_f10, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r,
D_Z_ter_i, Z_int_2_f10, D_Z_int_2_f10_r, D_Z_int_2_f10_i] =
Find_Zw_with_error10(f,Cond2_f10_r,D_Cond2_f10_r, Cond2_f10_i, D_Cond2_f10_i,
R_load, D_R_load, C_load, D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub,
D_R_sub, C_sub, D_C_sub);

[Z_w_2_l10, D_Z_w_2_l10_r, D_Z_w_2_l10_i, R_w_2_l10, D_R_w_2_l10,
C_w_2_l10, D_C_w_2_l10, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r,
D_Z_ter_i, Z_int_2_l10, D_Z_int_2_l10_r, D_Z_int_2_l10_i] =
Find_Zw_with_error10(f,Cond2_l10_r,D_Cond2_l10_r, Cond2_l10_i, D_Cond2_l10_i,
R_load, D_R_load, C_load, D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub,
D_R_sub, C_sub, D_C_sub);

[Z_w_3_40, D_Z_w_3_40_r, D_Z_w_3_40_i, R_w_3_40, D_R_w_3_40, C_w_3_40,
D_C_w_3_40, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r, D_Z_ter_i,
Z_int_3_40, D_Z_int_3_40_r, D_Z_int_3_40_i] = Find_Zw_with_error10(f,
Cond3_40_r, D_Cond3_40_r, Cond3_40_i, D_Cond3_40_i, R_load, D_R_load, C_load,
D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub, D_R_sub, C_sub, D_C_sub);

[Z_w_3_f20, D_Z_w_3_f20_r, D_Z_w_3_f20_i, R_w_3_f20, D_R_w_3_f20,
C_w_3_f20, D_C_w_3_f20, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r,
D_Z_ter_i, Z_int_3_f20, D_Z_int_3_f20_r, D_Z_int_3_f20_i] =
Find_Zw_with_error10(f,Cond3_f20_r,D_Cond3_f20_r, Cond3_f20_i, D_Cond3_f20_i,
R_load, D_R_load, C_load, D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub,
D_R_sub, C_sub, D_C_sub);

[Z_w_3_l20, D_Z_w_3_l20_r, D_Z_w_3_l20_i, R_w_3_l20, D_R_w_3_l20, C_w_3_l20, D_C_w_3_l20, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r, D_Z_ter_i, Z_int_3_l20, D_Z_int_3_l20_r, D_Z_int_3_l20_i] = Find_Zw_with_error10(f,Cond3_l20_r,D_Cond3_l20_r, Cond3_l20_i, D_Cond3_l20_i, R_load, D_R_load, C_load, D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub, D_R_sub, C_sub, D_C_sub);

[Z_w_3_f10, D_Z_w_3_f10_r, D_Z_w_3_f10_i, R_w_3_f10, D_R_w_3_f10, C_w_3_f10, D_C_w_3_f10, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r, D_Z_ter_i, Z_int_3_f10, D_Z_int_3_f10_r, D_Z_int_3_f10_i] = Find_Zw_with_error10(f,Cond3_f10_r,D_Cond3_f10_r, Cond3_f10_i, D_Cond3_f10_i, R_load, D_R_load, C_load, D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub, D_R_sub, C_sub, D_C_sub);

[Z_w_3_l10, D_Z_w_3_l10_r, D_Z_w_3_l10_i, R_w_3_l10, D_R_w_3_l10, C_w_3_l10, D_C_w_3_l10, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r, D_Z_ter_i, Z_int_3_l10, D_Z_int_3_l10_r, D_Z_int_3_l10_i] = Find_Zw_with_error10(f,Cond3_l10_r,D_Cond3_l10_r, Cond3_l10_i, D_Cond3_l10_i, R_load, D_R_load, C_load, D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub, D_R_sub, C_sub, D_C_sub);

[Z_w_4_40, D_Z_w_4_40_r, D_Z_w_4_40_i, R_w_4_40, D_R_w_4_40, C_w_4_40, D_C_w_4_40, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r, D_Z_ter_i, Z_int_4_40, D_Z_int_4_40_r, D_Z_int_4_40_i] = Find_Zw_with_error10(f, Cond4_40_r, D_Cond4_40_r, Cond4_40_i, D_Cond4_40_i, R_load, D_R_load, C_load, D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub, D_R_sub, C_sub, D_C_sub);

[Z_w_4_f20, D_Z_w_4_f20_r, D_Z_w_4_f20_i, R_w_4_f20, D_R_w_4_f20, C_w_4_f20, D_C_w_4_f20, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r, D_Z_ter_i, Z_int_4_f20, D_Z_int_4_f20_r, D_Z_int_4_f20_i] =

Find_Zw_with_error10(f,Cond4_f20_r,D_Cond4_f20_r, Cond4_f20_i, D_Cond4_f20_i, R_load, D_R_load, C_load, D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub, D_R_sub, C_sub, D_C_sub);

[Z_w_4_l20, D_Z_w_4_l20_r, D_Z_w_4_l20_i, R_w_4_l20, D_R_w_4_l20, C_w_4_l20, D_C_w_4_l20, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r, D_Z_ter_i, Z_int_4_l20, D_Z_int_4_l20_r, D_Z_int_4_l20_i] = Find_Zw_with_error10(f,Cond4_l20_r,D_Cond4_l20_r, Cond4_l20_i, D_Cond4_l20_i, R_load, D_R_load, C_load, D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub, D_R_sub, C_sub, D_C_sub);

[Z_w_4_f10, D_Z_w_4_f10_r, D_Z_w_4_f10_i, R_w_4_f10, D_R_w_4_f10, C_w_4_f10, D_C_w_4_f10, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r, D_Z_ter_i, Z_int_4_f10, D_Z_int_4_f10_r, D_Z_int_4_f10_i] = Find_Zw_with_error10(f,Cond4_f10_r,D_Cond4_f10_r, Cond4_f10_i, D_Cond4_f10_i, R_load, D_R_load, C_load, D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub, D_R_sub, C_sub, D_C_sub);

[Z_w_4_l10, D_Z_w_4_l10_r, D_Z_w_4_l10_i, R_w_4_l10, D_R_w_4_l10, C_w_4_l10, D_C_w_4_l10, Z_load, D_Z_load_r, D_Z_load_i, Z_ter, D_Z_ter_r, D_Z_ter_i, Z_int_4_l10, D_Z_int_4_l10_r, D_Z_int_4_l10_i] = Find_Zw_with_error10(f,Cond4_l10_r,D_Cond4_l10_r, Cond4_l10_i, D_Cond4_l10_i, R_load, D_R_load, C_load, D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub, D_R_sub, C_sub, D_C_sub);

b=[R_w_2_40,D_R_w_2_40,R_w_2_f20,D_R_w_2_f20,R_w_2_l20,D_R_w_2_l20,R_w_2_f10,D_R_w_2_f10,R_w_2_l10,D_R_w_2_l10];

a=[R_w_2_40,D_R_w_2_40,R_w_2_f20,D_R_w_2_f20,R_w_2_l20,D_R_w_2_l20,R_w_2_f10,D_R_w_2_f10,R_w_2_l10,D_R_w_2_l10,R_w_3_40,D_R_w_3_40,R_w_3_f20,D_R_w_3_f20,R_w_3_l20,D_R_w_3_l20,R_w_3_f10,D_R_w_3_f10,R_w_3_l10,D_R_

```
w_3_l10,R_w_4_40,D_R_w_4_40,R_w_4_f20,D_R_w_4_f20,R_w_4_l20,D_R_w_4_l2
0,R_w_4_f10,D_R_w_4_f10,R_w_4_l10,D_R_w_4_l10];

%Saving in a mat file
clear('Ch1','Ch2','Ch3','Ch4','Ch1r','Ch2r','Ch3r','Ch4r')
save(dataFile);
%Saving in a txt file
% dataDirectory = 'G:\Measurement\PCMUCONNK46\scope data\Die_64212\matlab
results\';
% fid = fopen([dataDirectory dataFile '.txt'],'w');
% fprintf(fid,'%9.2f \t %9.2f \t %9.2f \t %9.2f \t %9.2f \t %9.2f \t %9.2f \t %9.2f
\t %9.2f \t %9.2f \t %9.2f \t %9.2f \t %9.2f \t %9.2f \t %9.2f \t %9.2f \t %9.2f \t
%9.2f \t %9.2f \t %9.2f \t %9.2f \t %9.2f \t %9.2f \t %9.2f \t %9.2f \t %9.2f \t
%9.2f \t ',R_w_2_40, D_R_w_2_40, R_w_2_f20, D_R_w_2_f20, R_w_2_l20,
D_R_w_2_l20, R_w_2_f10, D_R_w_2_f10, R_w_2_l10, D_R_w_2_l10, R_w_3_40,
D_R_w_3_40, R_w_3_f20, D_R_w_3_f20, R_w_3_l20, D_R_w_3_l20, R_w_3_f10,
D_R_w_3_f10, R_w_3_l10, D_R_w_3_l10, R_w_4_40, D_R_w_4_40, R_w_4_f20,
D_R_w_4_f20, R_w_4_l20, D_R_w_4_l20, R_w_4_f10, D_R_w_4_f10, R_w_4_l10,
D_R_w_4_l10);
% fclose(fid);
```

5.5.2 Sinusoidal fit code

```
%-------------------(by Gokhan Bakan, Faruk Dirisaglik, Sadid Muneer)--------------------%
function [amplitude D_amplitude offset D_offset RMSE] = sine_fit_alt(data,
FittingPhase)
%for Comm tools of Matlab
V1      = data;
f       = 1e6;                  % applied sinusoidal frequency
Sc      = 5000;                 % samples per cycle
Cycles = 48;                    % cySces per step
```

```
Sst      = Sc*cycles;                % samples per step
t        = 0.2e-9*[1:Sst];           % time variable for all 48 cycles
V1_temp      = zeros(Sst*40,1);      %getting the size of V1 right
V1_temp(1:length(V1))= V1;
StepData     = reshape(V1_temp,Sst,40);
offset       = mean(StepData);
sine_mat     = repmat(sin(2*pi*f*t'+FittingPhase),1,40);
amplitude    = mean(2*sine_mat.*StepData);
RMSE         = sqrt(mean((StepData-repmat(offset,Sst,1)-
repmat(amplitude,Sst,1).*sine_mat).^2));
D_offset     = RMSE/sqrt(Sst);
D_amplitude  = RMSE*sqrt(2)/sqrt(Sst);
if FittingPhase ~= 0 && FittingPhase ~= pi/2
   figure
   plot(t,StepData(:,1))
   hold on
   plot(t,amplitude(1)*sin(2*pi*f*t+FittingPhase)+offset(1),'r')
   figure
   plot(t,StepData(:,19))
   hold on
   plot(t,amplitude(19)*sin(2*pi*f*t+FittingPhase)+offset(19),'r')
end
```

5.5.3 Real and imaginary components code

```
%----------------------(by Gokhan Bakan, Faruk Dirisaglik)-----------------------%
function [I_r D_I_r I_i D_I_i] = find_I10 (V_b_r, D_V_b_r, V_b_i, D_V_b_i, R_ter,
D_R_ter, C_ter, D_C_ter, f)

omeg   = 2*pi*f;                   % radian frequency
% find Z_ter and error
```

```
Z_ter          = (1/R_ter+1i*omeg*C_ter)^-1;
Z_ter_r        = real(Z_ter);
Z_ter_i        = imag(Z_ter);
D_Z_ter_r      = sqrt(((1-
omeg^2*C_ter^2*R_ter^2)*D_R_ter/(1+omeg^2*R_ter^2+C_ter^2)^2)^2+(2*omeg^2*
R_ter^3*C_ter*D_C_ter/(1+omeg^2*R_ter^2+C_ter^2)^2)^2);
D_Z_ter_i      =
sqrt((2*omeg*C_ter*R_ter*D_R_ter/(1+omeg^2*R_ter^2+C_ter^2)^2)^2+((omeg^3*C_
ter^2*R_ter^4-omeg*R_ter^2)*D_C_ter/(1+omeg^2*R_ter^2+C_ter^2)^2)^2);

V_b            = V_b_r + 1i*V_b_i;
I              = V_b/Z_ter;
I_r_check      = real(I);
I_i_check      = imag(I);

% find I_r I_i and errors

C_D    = Z_ter_r^2+Z_ter_i^2;              % Common denumerator

I_r            = (V_b_r*Z_ter_r + V_b_i*Z_ter_i)/C_D;
D_I_r          =
sqrt((Z_ter_r*D_V_b_r/C_D).^2+(Z_ter_i*D_V_b_i/C_D).^2+((V_b_r/C_D-
2*Z_ter_r*I_r/C_D)*D_Z_ter_r).^2+((V_b_i/C_D-2*Z_ter_i*I_r/C_D)*D_Z_ter_i).^2);

I_i            = (V_b_i*Z_ter_r - V_b_r*Z_ter_i)/(Z_ter_r^2+Z_ter_i^2);
D_I_i          =
sqrt((Z_ter_r*D_V_b_i/C_D).^2+(Z_ter_i*D_V_b_r/C_D).^2+((V_b_i/C_D-
2*Z_ter_r*I_i/C_D)*D_Z_ter_r).^2+((-V_b_r/C_D-2*Z_ter_i*I_i/C_D)*D_Z_ter_i).^2);
```

5.5.4 Linear regression with errors in X and Y code

```
%-------------(from http://www.mathworks.com/matlabcentral/fileexchange/26586-linear-regression-with-errors-in-x-and-y/content/york_curve_fit_0_01/york_fit.m)--------------%

function [a, sigma_a, b, sigma_b] = york_fit10(X,sigma_X,Y,sigma_Y,r)
%[a, b, sigma_a, sigma_b, b_save] = york_fit(X,Y,sigma_X,sigma_Y, r)
%Performs linear regression for data with errors in both X and Y, following the method in York et al.
%X,Y are row vectors of regression data.
%sigma_X and sigma_Y are row vectors or single values for the error in X and Y.
%r is a row vector or singal value for the correlation coefficeients between the errors.
%References:
%D. York, N. Evensen, M. Martinez, J. Delgado "Unified equations for the slope, intercept, and standard errors of the best straight line" Am. J. Phys. 72 (3) March 2004.
%Copyright Travis Wiens 2010 travis.mlfx@nutaksas.com

N_itermax      =10;                %maximum number of interations
Tol            =1e-15;             %relative tolerance to stop at
N              =numel(X);
 if nargin<5;
r         =0;
end
 if numel(sigma_X)==1
   sigma_X     =sigma_X*ones(1,N);
end
 if numel(sigma_Y)==1
   sigma_Y     =sigma_Y*ones(1,N);
end
 if numel(r)==1
   r           =r*ones(1,N);
end
```

```
 %make initial guess at b using linear squares
Tmp    =Y/[X; ones(1,N)];
b_lse   =tmp(1);
%a_lse=tmp(2);
 b       =b_lse;                          %initial guess
 omega_X=1./sigma_X.^2;
omega_Y=1./sigma_Y.^2;
 alpha  =sqrt(omega_X.*omega_Y);
 b_save          =zeros(1,N_itermax+1);        %vector to save b iterations in
b_save(1)=b;
 for i=1:N_itermax
    W    =omega_X.*omega_Y./(omega_X+b^2*omega_Y-2*b*r.*alpha);
     X_bar       =sum(W.*X)/sum(W);
    Y_bar        =sum(W.*Y)/sum(W);
     U    =X-X_bar;
    V     =Y-Y_bar;
     beta=W.*(U./omega_Y+b*V./omega_X-(b*U+V).*r./alpha);

    b     =sum(W.*beta.*V)/sum(W.*beta.*U);
    b_save(i+1)=b;
    if abs((b_save(i+1)-b_save(i))/b_save(i+1))<tol
       break
    end
end
 a       =Y_bar-b*X_bar;
 x       =X_bar+beta;
%y=Y_bar+b*beta;
 x_bar=sum(W.*x)/sum(W);
%y_bar=sum(W.*y)/sum(W);
 u       =x-x_bar;
%v=y-y_bar;
```

```
 sigma_b        =sqrt(1/sum(W.*u.^2));
sigma_a         =sqrt(1./sum(W)+x_bar^2*sigma_b^2);
```


5.5.5 Wire impedance code

```
%-----------------------(by Gokhan Bakan, Faruk Dirisaglik)-----------------------%
function [Z_w, D_Z_w_r, D_Z_w_i, R_w, D_R_w, C_w, D_C_w, Z_load, D_Z_load_r,
D_Z_load_i, Z_ter, D_Z_ter_r, D_Z_ter_i, Z_int, D_Z_int_r, D_Z_int_i] =
Find_Zw_with_error10(f,Cond_r,D_Cond_r, Cond_i, D_Cond_i, R_load, D_R_load,
C_load, D_C_load, R_ter, D_R_ter, C_ter, D_C_ter, R_sub, D_R_sub, C_sub,D_C_sub)
omeg = 2*pi*f;          % radian frequency
%finds total impedance (sum of impedances of load, termination and the
%wire) and errors in real and imaginary components of it. Inputs are
```

```
%conductance (both real and imaginary) and errors in both real and imaginary
%conductances as outputted by the linear regression function.
Z_t      = 1/(Cond_r+1i*Cond_i);
D_Z_t_r = sqrt(((Cond_i^2-
Cond_r^2)*D_Cond_r/(Cond_i^2+Cond_r^2)^2)^2+(2*Cond_i*Cond_r*D_Cond_i/(Con
d_i^2+Cond_r^2)^2)^2);
D_Z_t_i          = sqrt(((Cond_r^2-
Cond_i^2)*D_Cond_i/(Cond_i^2+Cond_r^2)^2)^2+(2*Cond_i*Cond_r*D_Cond_r/(Con
d_i^2+Cond_r^2)^2)^2);
%load impedance and error
Z_load           = (1/R_load+1i*omeg*C_load)^-1;
D_Z_load_r = sqrt(((1-
omeg^2*C_load^2*R_load^2)*D_R_load/(1+omeg^2*R_load^2*C_load^2)^2)^2+(2*o
meg^2*R_load^3*C_load*D_C_load/(1+omeg^2*R_load^2*C_load^2)^2)^2);
D_Z_load_i =
sqrt((2*omeg*C_load*R_load*D_R_load/(1+omeg^2*R_load^2*C_load^2)^2)^2+((ome
g^3*C_load^2*R_load^4-
omeg*R_load^2)*D_C_load/(1+omeg^2*R_load^2*C_load^2)^2)^2);
%termination impedance and error
Z_ter    = (1/R_ter+1i*omeg*C_ter)^-1;
D_Z_ter_r = sqrt(((1-
omeg^2*C_ter^2*R_ter^2)*D_R_ter/(1+omeg^2*R_ter^2*C_ter^2)^2)^2+(2*omeg^2*R
_ter^3*C_ter*D_C_ter/(1+omeg^2*R_ter^2*C_ter^2)^2)^2);
D_Z_ter_i =
sqrt((2*omeg*C_ter*R_ter*D_R_ter/(1+omeg^2*R_ter^2*C_ter^2)^2)^2+((omeg^3*C_t
er^2*R_ter^4-omeg*R_ter^2)*D_C_ter/(1+omeg^2*R_ter^2*C_ter^2)^2)^2);
%intermadiate impedance
Z_int    = Z_t-Z_load-Z_ter;
Z_int_r          = real(Z_int);
Z_int_i          = imag(Z_int);
D_Z_int_r = D_Z_t_r+D_Z_load_r+D_Z_ter_r;
```

```
D_Z_int_i = D_Z_t_i+D_Z_load_i+D_Z_ter_i;
%substrate impedance
Z_sub  = R_sub - 1i/omeg/C_sub;
Z_sub_r = real(Z_sub);
Z_sub_i = imag(Z_sub);
D_Z_sub_r = D_R_sub;
D_Z_sub_i = D_C_sub/omeg/C_sub^2;
% wire impedance and error calculation
Z_w = Z_sub*Z_int/(Z_sub-Z_int);
Z_temp = Z_sub-Z_int;                          %denumerator of Z_w
Z_temp_r = real(Z_temp);
Z_temp_i = imag(Z_temp);
D_Z_temp_r = D_Z_sub_r + D_Z_int_r;
D_Z_temp_i = D_Z_sub_i + D_Z_int_i;

Z_temp2 = Z_sub*Z_int;                         % numerator of Z_w;
Z_temp2_r = real(Z_temp2);
Z_temp2_i = imag(Z_temp2);
D_Z_temp2_r =
sqrt((D_Z_sub_r*Z_int_r)^2+(Z_sub_r*D_Z_int_r)^2+(D_Z_sub_i*Z_int_i)^2+(Z_sub_
i*D_Z_int_i)^2);
D_Z_temp2_i =
sqrt((D_Z_sub_i*Z_int_r)^2+(Z_sub_i*D_Z_int_r)^2+(D_Z_sub_r*Z_int_i)^2+(Z_sub_
r*D_Z_int_i)^2);

Z_temp3 = conj(Z_temp)*Z_temp2;  % multiplication of numerator and denumerator of
Z_w;
Z_temp3_r_check = real(Z_temp3);
Z_temp3_i_check = imag(Z_temp3);
Z_temp3_r = Z_temp2_r*Z_temp_r+Z_temp2_i*Z_temp_i;
Z_temp3_i = Z_temp2_i*Z_temp_r-Z_temp_i*Z_temp2_r;
```

```
D_Z_temp3_r =
sqrt((D_Z_temp2_r*Z_temp_r)^2+(Z_temp2_r*D_Z_temp_r)^2+(D_Z_temp2_i*Z_tem
p_i)^2+(Z_temp2_i*D_Z_temp_i)^2);
D_Z_temp3_i =
sqrt((D_Z_temp2_i*Z_temp_r)^2+(Z_temp2_i*D_Z_temp_r)^2+(D_Z_temp_i*Z_temp2
_r)^2+(Z_temp_i*D_Z_temp2_r)^2);

Z_w_r = real(Z_w);
Z_w_i = imag(Z_w);
Z_w_check = (Z_temp3_r + 1i*Z_temp3_i)/(Z_temp_r^2+Z_temp_i^2);

C_D = Z_temp_r^2+Z_temp_i^2;                %Common denumerator
D_Z_w_r =
sqrt((D_Z_temp3_r/C_D)^2+(2*Z_temp3_r*Z_temp_r*D_Z_temp_r/C_D^2)^2+(2*Z_te
mp3_r*Z_temp_i*D_Z_temp_i/C_D^2)^2);
D_Z_w_i =
sqrt((D_Z_temp3_i/C_D)^2+(2*Z_temp3_i*Z_temp_r*D_Z_temp_r/C_D^2)^2+(2*Z_te
mp3_i*Z_temp_i*D_Z_temp_i/C_D^2)^2);

% wire impedance and error calculation
R_w = Z_w_r*(1+Z_w_i^2/Z_w_r^2);
D_R_w = sqrt(((1-Z_w_i^2/Z_w_r^2)*D_Z_w_r)^2 + (2*Z_w_i*D_Z_w_i/Z_w_r)^2);
C_w = -Z_w_i/(Z_w_r*R_w*omeg);
D_C_w =
sqrt((Z_w_i*D_Z_w_r/(R_w*omeg*Z_w_r^2))^2+(D_Z_w_i/(R_w*omeg*Z_w_r))^2+(
Z_w_i*D_R_w/(R_w^2*omeg*Z_w_r))^2);
```

5.6 Measured resistivity values

Table 5.11 Measured liquid, crystalline (hcp and fcc), and amorphous GST average resistivity values.

Phase		Liquid GST		Crystalline (hcp) GST				Crystalline (fcc) GST					Amorphous GST				
Technique		During the pulse AC high-speed		DC *I-V*	baseline	AC high-speed		Annealed @ 425 K	Annealed @ 450 K	Annealed @ 500 K	DC *I-V*	AC high-speed	DC *I-V*	Stepping up AC high-speed		Stepping down AC high-speed	
		ρ	±	ρ	ρ	ρ	±	ρ	ρ	ρ	ρ	±	ρ	ρ	±	ρ	±
		(μΩ.cm)		(μΩ.cm)				(mΩ.cm)					(mΩ.cm)				
Temperature (K)	300	130.0	63.2	1020.0	1150.0	1130.0	663.2	78.2	21.1	5.0			96439.3	99512.8	47620.7	99690.3	47936.6
	325													50086.6	19379.9	50031.9	19026.9
	330							65.7									
	335								19.2								
	350	149.0	41.1	1350.0	1460.0	1500.0	486.6			4.6			29247.0	28336.7	11467.9	28279.1	11303.3
	360							54.6									
	370								16.7								
	375													16946.9	3931.3	17136.3	4424
	390							45.4									
	400	173.8	42.8	1220.0	1360.0	1360.0	534.1		14.9	4.1			7867.5	10330.1	4772.8	10293.8	4812.1
	425							32.6						6288.9	1407.1	6317.9	1579.5
	450	226.3	64.1	1330.0	1420.0	1300.0	372.8		12.5	3.7				4035.5	1392.1	3907.3	1371.6
	475													2333.5	793.5	2237.6	742.9
	500	280.2	82.7	1340.0	1460.0	1470.0	412.7			3.6				1367.4	699.3	1050.6	823.0
	525													884.5	528.1	649.7	512.2
	550	308.8	51.0	1250.0	1380.0	1430.0	343.5				63.8	26.5		568.8	462.9		
	575										49.7	19.8		324.0	127.0		
	600	341.3	61.1	1220.0	1310.0	1370.0	355.1				39.4	10.3		191.0	16.2		
	625										31.3	10.4					
	650	396.6	86.7	1130.0	1160.0	1150.0	237.0				24.6	7.7					
	675	402.4	65.1	1210.0	1220.0	1230.0	373.1				19.7	5.6					

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